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A High Speed Combinational-logic Shifter using Threshold Logic Technology

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ABSTRACT
In this work the concentration of attention is to create a High Speed Combinational-logic Shifter depending upon the principle of threshold logic gates (TLG). After fixing the threshold logic gates required for our work, we have implemented different gates/circuits made up of different elements like tunnel junctions and capacitances. The gates or circuits designed or implemented are the modified version of a multi-input threshold logic gate. For constructing the logic circuits, we have a glance over a generic threshold gate with which a logic gate like 3-input AND, 4-input OR and other more complex linear logic circuitswhich are having many inputs but one output can be constructed. By means of a 3-input AND, 4-input OR and 4:1 Multiplexer, we have been able to construct a complex circuit called 4-bit Combinational-logic Shifter. For the verification purpose, the threshold logic gate based Combinational-logic Shifter is converted into capacitor- and tunnel junction-based device which has been verified by the simulator SIMON and found that the input-output relationship results are matching with the theoretical analysis. As the linearly separable TLGs are easy to implement, so the gates we have made up are tested whether they are linearly separable or not. How many elements needed to construct a particular gate or circuit are measured. Switching or processing delay for executing a function in a gate/ circuit is measured also. Power consumption for each element is taken into consideration. The curves in connection with Delay vs. Error Probability and Delay vs. capacitance are shown. Processing delays between CMOS based circuits and TLG are compared and realized that TLG based circuit are having higher speed than CMOS basedcircuit.
Keywords: *High speed, Threshold-logic, tunneling, generic logic gate, combinational shifter*

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I. Introduction

Using sequential circuit we are able to implement a right shift or left-shift register. In this work, we have constructed a Combinational-logic Shifter which performs left-shift or right-shift operation under the control of the selection lines. A shifter may consist of n-stages for a system having n-parallel lines under the control of $log_2(n)$ control lines. For space limitation, we have made up of a shifter of 4-stages. We have followed the principle of threshold logic whenever a logic circuit is built. The principle is: when theweighted sum of the inputs of a logic gate is greater than or equal to the threshold valueθ of the gate/circuit concerned then the output logic is $high$ otherwise low. A logical circuit called inverter is also provided for the purpose of inverting the value of a desired signal. In sections 2, 3, 4 and 5 some logic gates are constructed after analyzing their properties. In section 5, a LTG based 4:1 Multiplexer is discussed and the desired diagram for a Combinational-logic Shifter is elaborately discussed in section 6.

II. 3-input AND gate

Threshold logic equation of a 3-input AND gate of three variables X_1, X_2 and X_3 will be like

$F(X_1X_2X_3) = \text{sgn}(w_1X_1 + w_2X_2 + w_3X_3 - \theta)$ …….. (1)

For finding the threshold logic equation of 3-input AND ($F= X_1X_2X_3$), the logic variables (X_1, X_2 and X_3) for positive logic will be set as 1 each.The equation (1) will be as

$F = sgn(w_1 + w_2 + w_3 - \theta)$ ……..(2)

To obtain the values of w_1 , w_2,w_3 and θ, we first draw the truth table Table-1 of a 3-input AND gate and compare the weighted sum of weights w_1, w_2, and $w_3$of three variables X_1 and X_2 and X_3respectively with the

threshold value θ [1,2,3, 7, 9].

Table-1

X_1	X_2	X_3	F=$X_1X_2X_3$	θ	Eqn. No.
0	0	0	0	$0<\theta$	(1)
0	0	1	0	$w_3 < \theta$	(2)
0	1	0	0	$w_2 < \theta$	(3)
0	1	1	0	$w_2 + w_3 < \theta$	(4)
1	0	0	0	$w_1 < \theta$	(5)
1	0	1	0	$w_1 + w_3 < \theta$	(6)
1	1	0	0	$w_1 + w_2 < \theta$	(7)
1	1	1	1	$w_1 + w_2 + w_3 \geq \theta$	(8)

For positive logic, we assume weights of X_1, X_2 and X_3 are positive 1 each i.e. w_1=1, w_2=1 and w_3=1. For the case of threshold "θ", if we take the value θ =3, then all the eight inequalities in right-most column in Table-1 are satisfied. So we get a solution set for $\{w_1, w_2, w_3: \theta\}$={1,1,1:3}. So the Threshold logic equation for 3-input AND gate is given in equation (1) can be written as equation (3). The corresponding threshold logic gate is drawn in Fig. 1.

$F(X_1X_2X_3) = sgn(X_1 + X_2 + X_3 - 3)$ .....(3)

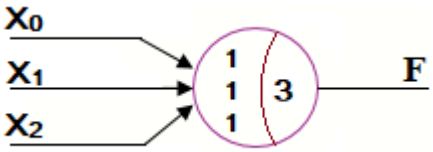


Fig. 1TLG of F = $X_1X_2X_3$

III. 4-input OR Gate

Now we will consider about 4-input OR gate. Let the threshold logic equation of a 4-input OR gate of four variables X_1, X_2, $X_3$and X_4be

$Y(X_1X_2X_3X_4) = sgn(w_1X_1 + w_2X_2 + w_3X_3 + w_4X_4 - \theta)$ .....(4)

For finding the threshold logic equation of4-input OR gate, logic variables (X_1, X_2, $X_3$and X_4) for positive logic will be set as 1 each.The equation (4) will be as

$Y = sgn(w_1 + w_2 + w_3 + w_4 - \theta)$ ..... (5)

To obtain the values of $w_1, w_2, w_3, w_4$and θ, we first draw the truth table Table-2 of a 4-input OR gate and compare the weighted sum of weights w_1,w_2,and$w_3$of four variables X_1 and X_2, $X_3$and X_4respectively with the threshold value θ [1,2,3, 8, 9].

Table-2

X_1	X_2	X_3	X_4	F=$X_1X_2X_3$	θ	inequality No.
0	0	0	0	0	$0<\theta$	(1)
0	0	0	1	1	$w_4 \geq \theta$	(2)
0	0	1	0	1	$w_3 \geq \theta$	(3)
0	0	1	1	1	$w_3 + w_4 \geq \theta$	(4)
0	1	0	0	1	$w_2 \geq \theta$	(5)
0	1	0	1	1	$w_2 + w_4 \geq \theta$	(6)
0	1	1	0	1	$w_2 + w_3 \geq \theta$	(7)
0	1	1	1	1	$w_2 + w_3 + w_4 \geq \theta$	(8)
1	0	0	0	1	$w_1 \geq \theta$	(9)
1	0	0	1	1	$w_1 + w_4 \geq \theta$	(10)
1	0	1	0	1	$w_1 + w_3 \geq \theta$	(11)
1	0	1	1	1	$w_1 + w_3 + w_4 \geq \theta$	(12)
1	1	0	0	1	$w_1 + w_2 \geq \theta$	(13)

1	1	0	1	1	$w_1 + w_2 + w_4 \geq \theta$	(14)
1	1	1	0	1	$w_1 + w_2 + w_3 \geq \theta$	(15)
1	1	1	1	1	$w_1 + w_2 + w_3 + w_4 \geq \theta$	(16)

From the inequality (1), we have θ is a positive number and from inequalities (2), (3), (5) and (9) we conclude that w_1 , w_2,w_3, w_4 are all positive as $\theta > 0$. If we assume that w_1=1, w_2=1, $w_3 = 1$,w_4=1 and $\theta = 1$, then all the sixteen inequalities in right-most column in Table-2 are satisfied. So we get a solution set for $\{w_1$, w_2,w_3, w_4: θ} = {1, 1,1,1:1}. So the Threshold logic equation for 4-input OR gate is given in equation (4) can be written as equation (6). The corresponding threshold logic gate is drawn in Fig. 2.

$Y(X_1X_2X_3X_4) = sgn\,(X_1 + X_2 + X_3 + X_4 - 1)$ ……..(6)

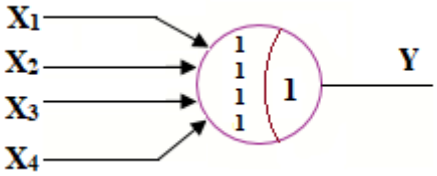


Fig. 2TLG of $Y = X_1 + X_2 + X_3 + X_4 - 1$

IV. Inverter

An inverter shown in Fig.3(a)[1-4, 8-10] is made up of 9 elements: 4 Tunnel junctions, 5 true capacitors; one bias or supply voltage V_s,one input terminal and one output terminal. This set of inverter is considered to constructed with two single electron transistors (SETs) connected in series. Upper two Tunnel junctions (J_1,J_2) and two true capacitors(C_g, C_b) comprise SET1. Similarly, The lower two Tunnel junctions (J_3, J_4) and two true capacitors (C_g, C_b) comprise SET2.Two inputsterminals connected to the same values V_{in} are straight coupled to the islands (small circles)of the SET1 and SET2 [1, 2, 8-10] through two capacitors C_g and C_g respectively. The island sizes of each SET are of sizeclose to 10 nm diameter of gold and their corresponding capacitor valueswill be less than 10aF. The output terminal V_0 directly connect the common channel in between SET_1 and SET_2.The output terminal is also grounded through a load capacitor C_L to suppress charging effects. When an inverter is used we choose the parameter values as:V_{g1}=0, V_{g2}=0.1× $\frac{q_e}{C}$, $C_L = 9C$, $C_j = \frac{1}{10}C$, $5C_j = \frac{1}{2}C$, $C_g = \frac{1}{2}C$,$C_b = \frac{17}{4}C$R$_j$50KΩ. For the case of simulation, the value of C =1aF is taken.

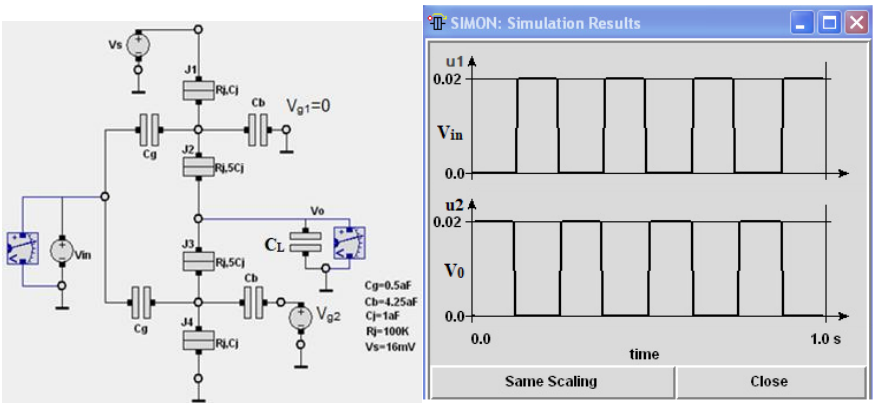


Fig. 3(a) Simulation set of an Inverter Fig.3 (b) input and output result after simulation of inverter

We keep the voltages $V_{g1} = 0$ *and* V_{g2}=16mV.The operation of the invertercan be described as: - the output V_0value will be 1 (logic high)if we set the input voltage V_{in} low and that will be 0 (logic low)ifwe set the input voltage V_{in} high. SET_1(upper part) will be in conduction modeand the SET_2 is in Coulomb blockade [2-4, 11]when the input signal V_{in} is set to low. This causes the output voltage $V_0$to connect to V_b and therefore the output voltage becomes high.If theinput voltage becomes high (logic 1), then the induced charges on each of the islands (for two SETs) are shifted by a fraction of an electron charge. As a result, SET_1goes in Coulomb blockade mode and the SET_2 in conducting condition. Then it is said that the output V_0changes the condition from high to low (logic 0).

In this work, we use the logic inputs "0" =0 Volts and logic "1"=0.1$\times \frac{q_e}{C}$.

For the case of simulation,we assume that C=1aF and Logic "1"= $0.1\times \frac{1.602\times10^{-19}}{1\times10^{-18}}= 0.1 \times 1.602 \times 10-2=16.02\times10-3=16.02 \cong 16$ mV.

V. General Purpose Multiple input threshold logic gate

A multiple threshold logic gate [1-10] depicted in Fig.4comprises a tunnel junction having internal capacitance C_j and resistanceR_j, two multi-input-signals (i) V_k^Ps and (ii) V_l^ns connected at two points 'q' and 'p' respectively. Each input voltage V_k^P (upper side) is connected to the point "q" through the capacitanceC_k^P ; and each input voltageV_l^n(lower side), is joined at the point "p" through the capacitance C_l^n. The bias voltage V_b, for the helping of the tunneling,is connected to the point "q" through the capacitor C_b. Tunnel Junction capacitor C_j is connected in between "p" and "q". Point "p" isgroundedthrough C_0.$C_j$and C_0 play the mail role in the circuit. For a LTG, the operation of it can be expressed by means of a function called$signun\ function$.The $signun\ function$of h(x) expressed by equations (7a) and (7b).

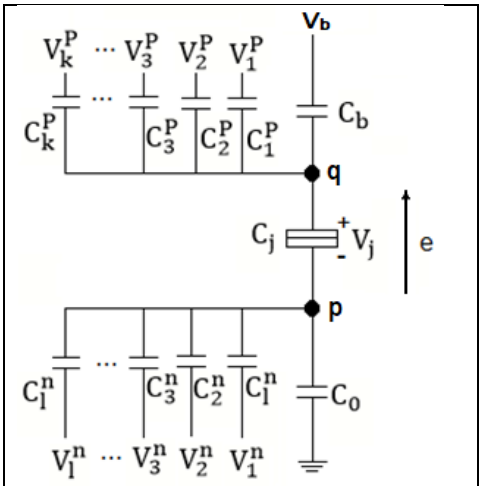


Fig. 4 Threshold logic gate with multi-input

$$g(x) = \text{sgn}\{h(x)\} = \begin{cases} 0, & if\ h(x) < 0 \\ 1, & if\ h(x) \geq 0 \end{cases} \quad \text{(7a)}$$

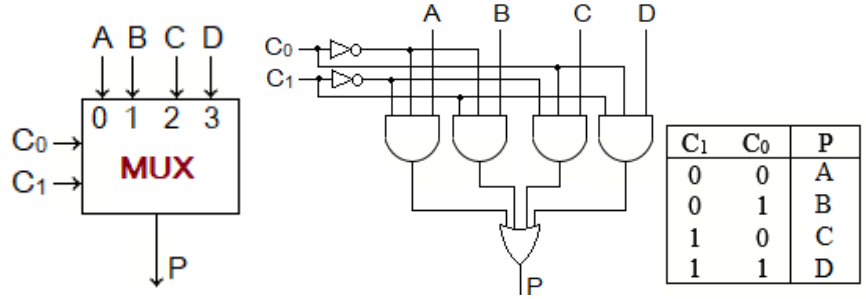
$$h(x) = \sum_{k=1}^{n}(w_k \times x_k) - \theta \quad \text{(7b)}$$

where $x_k$represents n-Boolean inputs, and w_k are their corresponding integer weights.

The LTG compares the threshold valueθwith the weighted sum of the inputs $\sum_{k=1}^{n}(w_k \times x_k)$. When $\sum_{k=1}^{n}(w_k \times x_k)$ is greater than or equal to the threshold value θ of the circuit then output of the LTG indicates high (logical "1"), otherwise low (logical "0").

VI. 4:1 Multiplexer

A 4:1 Multiplexer has four inputs, one output and two control lines. Block diagram of this Multiplexer is given in Fig. 5(a) where A, B, C and D are four inputs; C_0 and C_1 are two control lines and P is the one output line. Fig. 5(b) is the logic diagram and 5(c) is the functional diagram of 4-to-1line Multiplexer.



C_1	C_0	P
0	0	A
0	1	B
1	0	C
1	1	D

(a) Block diagram (b) Logic diagram (c) Functional diagram

Fig.5: 4-to-1line Multiplexer

6.1 Threshold logic gate based 4:1 Multiplexer

In the previous sections we have enlightened about the 3-input AND gate, 4-inpur OR gate and inverter. Following the logic diagram of Fig.5 (b), a threshold logic gate based 4-to-1 line Multiplexer is depicted in Fig.6.

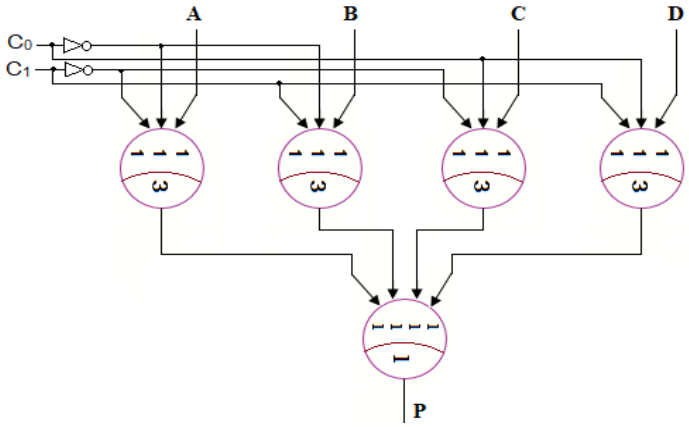


Fig.6 A Threshold logic gate based 4:1 Multiplexer

6.2 Combinational-logic shifter

With the help of four Threshold logic gate based 4:1 Multiplexers, we will be able to construct a 4-bit combinational-logic shifter and it is shown in Fig.7. In this circuit there are two control lines C_0 and C_1 which are connected to all four Multiplexers. These control lines help select the type of operations F_1, F_2, F_3 or F_4 of the shifter. The operations performed under the control of control lines C_0 and C_1 will be as:

When C_1 C_0 = 0 0, there will be no shift execution and only signal pass from F to the P lines directly.

When C_1 C_0 = 0 1, the control lines cause a right shift operation.

When C_1 C_0 = 1 0, the control lines cause a left shift operation.

When C_1 C_0 = 1 1, each multiplexer in the shifterchoose the line connected to 0 and as a result the P outputs will be equal to 0 each. The operations are listed in Table-3.

Table-3

C_1	C_0	operation	remark
0	0	P←F	No shift, only transfer F to P
0	1	P← shift-R	Right shift F into P
1	0	P← shift-L	Left shift F into P
1	1	P← 0	only transfer 0's into P

The circuit shown in Fig. 7 shows four stages of the combinational-logic shifter but can be increased for n-stages for a system with n-number of parallel lines. The input*Right input*serves as serial inputs for the stage-4 situated at the leftmost position and the*Left input* serves as serial inputs for the stage-1 situated at the rightmost position during the right-shift and left-shift respectively.

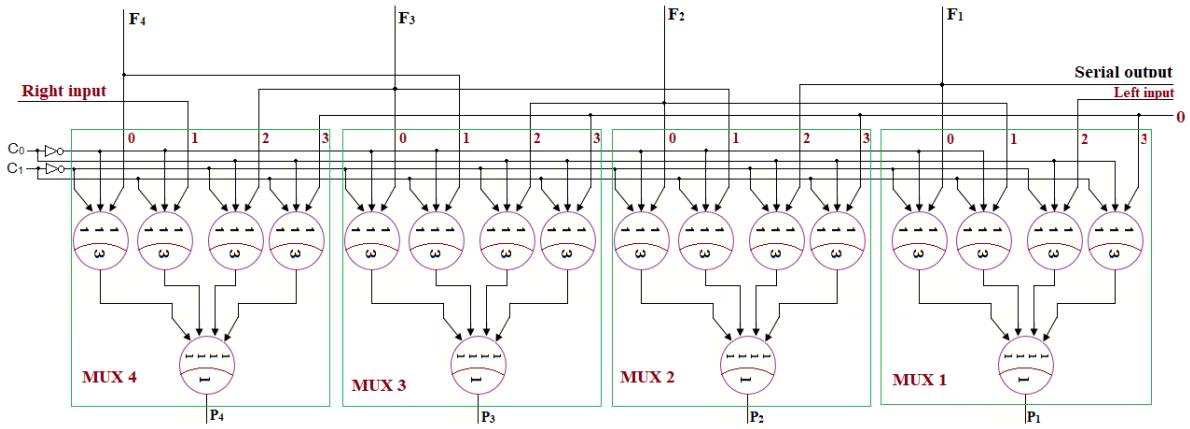


Fig. 7 A 4-bit combinational-logic shifter using TLGs

6.3 Simulation set and result of 4-bit combinational-logic shifter

For simulation set we need some components like registers and capacitors with their values. We are to find out them.We have analyzed the threshold logic expressions. After analyzing them, the corresponding parameters being required are measured and found out to implement the components like 4:1 Multiplexer and

combinational-logic shifter. The list of parameters relevant to theMultiplexer and combinational-logic shifterare given in Table-4.

Table-4

Sl. No.	Expressions used	Name of Expression	Parameters required for setting
1	$F(X_1X_2X_3) = sgn(X_1 + X_2 + X_3 - 3)$	3-input AND gate	logic input "0"=0V, logic "1" = 16mV,C=1aF, $C_1^P = C_2^P = C_3^P = \frac{1}{2}C$ =0.5aF, $C_b = 8.5aF$, $C_j = 0.25aF$, $C_L = 9aF, C_0 10aF$, R_j=$10^5\Omega$,. $V_b = V_b$ =V_s=16mV
2	$Y(X_1X_2X_3X_4) = sgn(X_1 + X_2 + X_3 + X_4 - 1)$	4-input OR gate	"0"=0V, logic "1" = 16mV,C=1aF, $C_1^P = C_2^P = C_3^P = C_4^P = \frac{1}{2}C$ =0.5aF, $C_b = 8aF$, $C_j = 0.25aF$, $C_L = 9aF, C_0 = 10aF$, R_j=$10^5\Omega$,. $V_b = 15.81mV$ V_b =V_s=16mV
3	$Y \leftarrow \overline{Y}$	Inverter	For the inverter, the parameter values chosen are:V_{g1}=0, V_{g2}=0.1× $\frac{q_e}{C}$, $C_L = 9C$,$C_j = \frac{1}{10}C$, $5C_j = \frac{1}{2}C$, $C_g = \frac{1}{2}C$,$C_b = \frac{17}{4}C$, R_j =50KΩ. For the case of simulation, the value of C =1aF is taken.

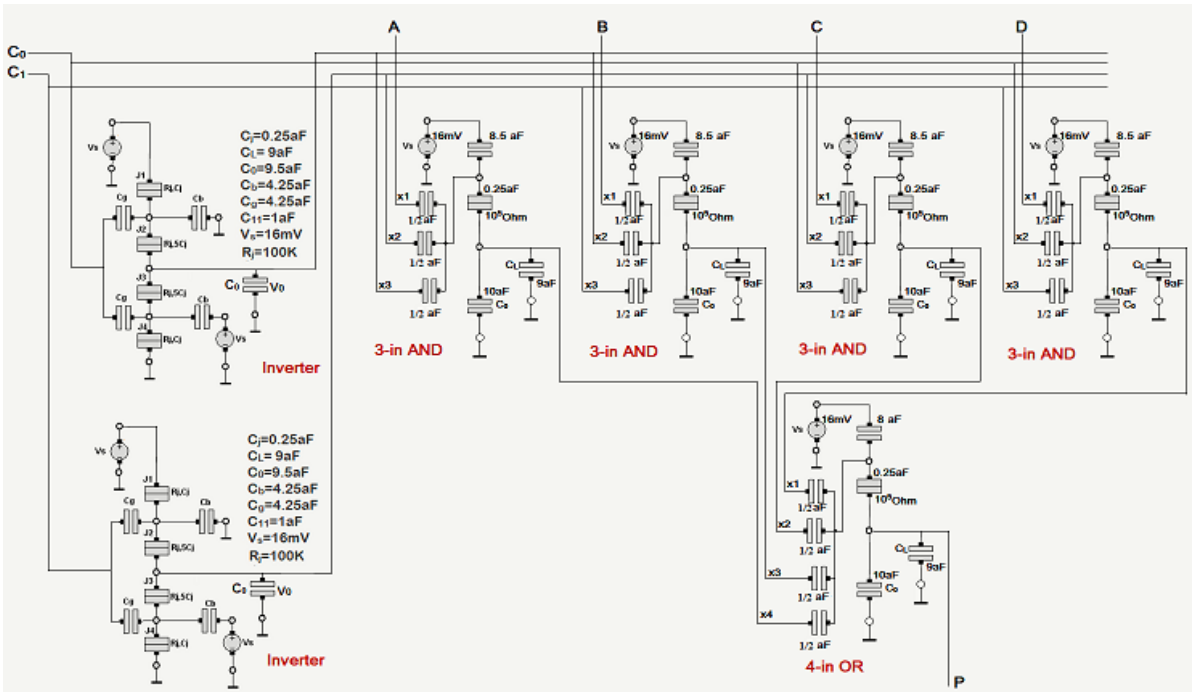


Fig.8 Simulation set of a 4:1 Multiplexer

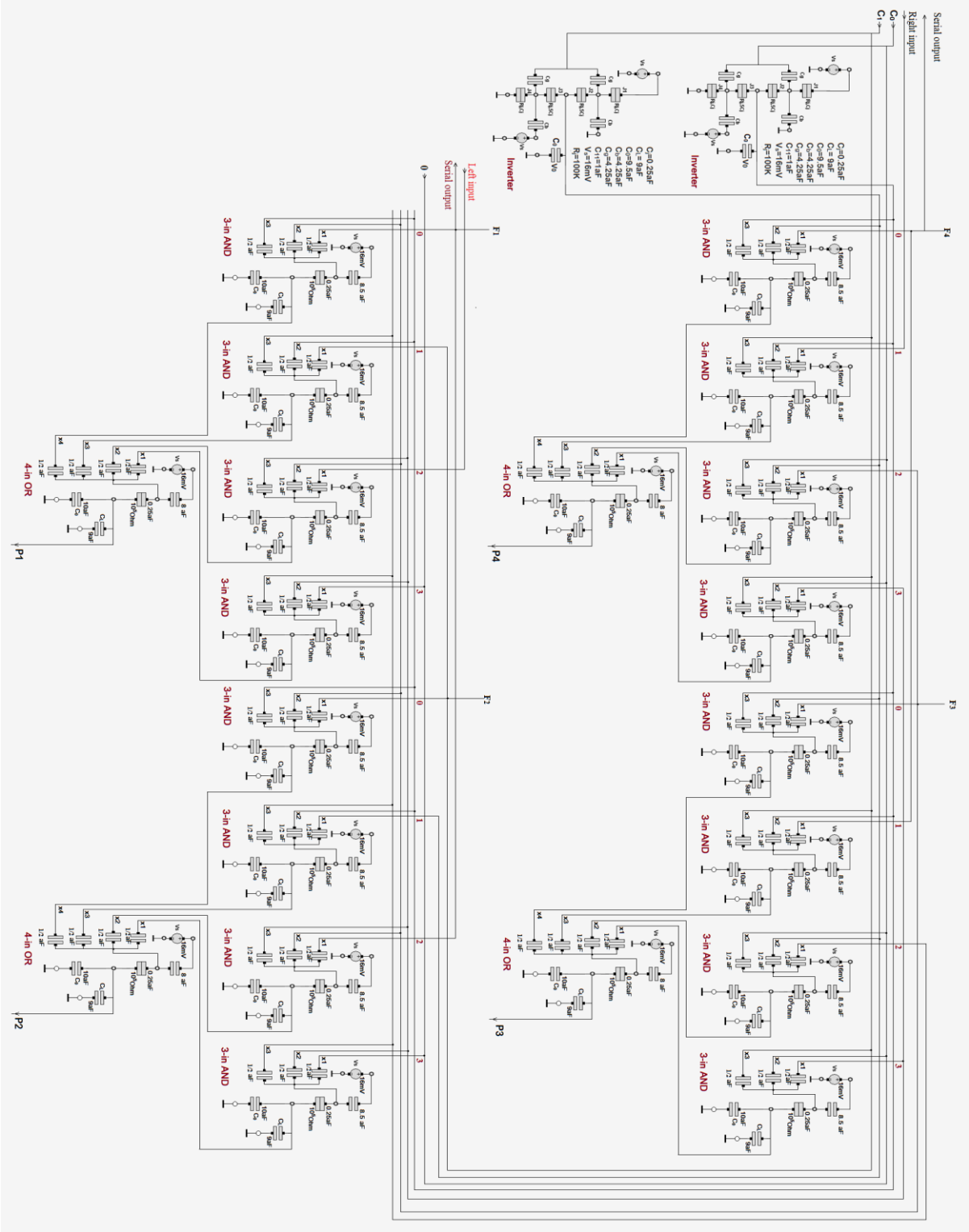


Fig. 9 Simulation set of a 4-bit combinational-logic shifter

When we want to varify the result of the 4-bit combinational-logic shifter discussed above for the Fig.9, we assume that $F_4F_3F_2F_1$ = 1011, Right input =1 and Left input = 0. Now, we put the control line input C_1C_0 =00, the output at the output terminals $P_4P_3P_2P_1$will be the same as $F_4F_3F_2F_1$, so $P_4P_3P_2P_1$=1011.

Next, when C_1C_0 is changed to 01, one right shift happens and the result becomes $P_4P_3P_2P_1$=1101, next when C_1C_0 is changed to 10, one left shift of $F_4F_3F_2F_1$happens and the result becomes $P_4P_3P_2P_1$=0110, and al last when C_1C_0 is changed to 11, all the four Multiplexers select the lines giving the value 0, so the result becomes $P_4P_3P_2P_1$=0000. The simulated results are depicted in Fig,10.The results are also given in Table-5 as well.

Table-5

Right input	**Left input**	**F_4**	**F_3**	**F_2**	**F_1**	
1	0	1	0	1	1	
C_1	**C_0**	**P_4**	**P_3**	**P_2**	**P_1**	**Result**
0	0	1	0	1	1	No change
0	1	1	1	0	1	Right shift F into P
1	0	0	1	1	0	Left shift F into P
1	1	0	0	0	0	0-line select

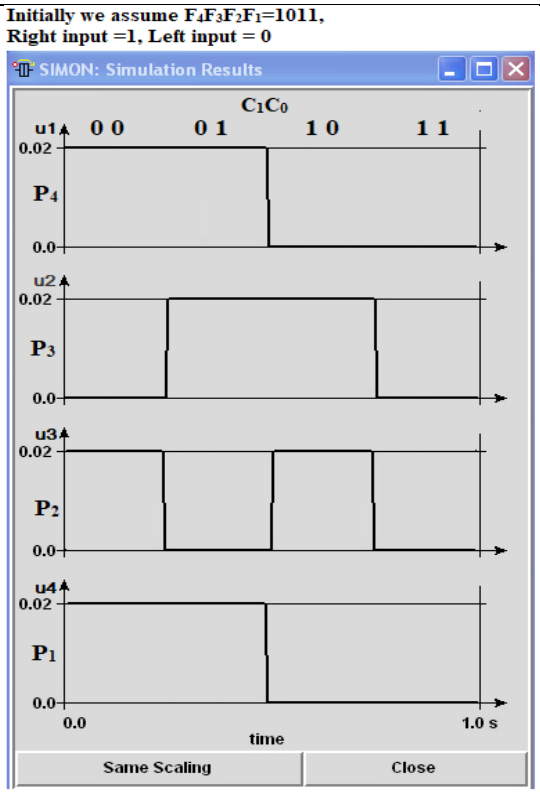


Fig.10 Simulation result of a 4-bit combinational-logic shifter

VII. Discussion apropos of Delay, Switching energy and Fastness

When we are analyzing the circuit of a device, it must have some components that are indispensable.Similarly, for the case of a shifter, 3-input AND gate, 4-input OR gate, 4:1 Multiplexer and inverter are essential. A 4-bit combinational-logic shifter is constructed by using the above sited components. Efficiency of a device depends upon the factors like execution time, required components, costs of materials, fan-outs, speed, power consumption etc. First we consider the processing delays of all the components used. Whenever anybody wants to calculate the processing/switching delays, he must involve the critical voltage $V_c$and the tunnel junction capacitanceC_j of the linear TLG. This delays as respects tologic gate/circuit can be measured by the approaches [1-3, 8, 9]shown as below:

Delay = $-(e|\ln(P_{error})|R_t) / (|V_j| - V_c)$ ..... (8)

Here,$V_j$represents the junction voltage and $V_c$becomes the critical voltage and R_t is the internal junction resistance.

Execution of the circuit will happens only when a tunneling event occurs. The tunneling event occurswhenever the tunnel junction voltage$V_j$is higher than or equal to the internal critical voltageV_c, i.e., when$|V_j| \geq V_c$. Whenever this conditional expression is gratified by a 2-input NOR gate, junction voltage of the 2-input NOR gate becomesV_j =11.8mV, the internal critical voltage V_c of the tunnel junction is found to be 11.58mV. The parameter values of tunnel resistance $R_t = 10^5\Omega$ and the probability of error $P_{error} = 10^{-12}$are given.Putting these values into equation (8) we measure the gate delay =0.062|ln(P_{error}) |ns = 2.21ns. In this same way we have found out the delays of different gates/ circuits and they are listed in Table-6.

At the time of tunneling, an electron goes through the junction barrier, the total energy in the circuit is changed. The energy levels,in the circuit concerned, before and after the tunneling event are calculated using the equation (9).

$$\Delta E = E_{before\ tunnel} - E_{after\ tunnel}$$
$$= -e(V_c - |V_j|) \quad \text{..... (9)}$$

This is the switching/tunneling energy $-e(V_c - |V_j|)$that is consumed as soon as a tunnel event occurs in the tunneling circuit. Here we have listed the energy consumptions for different TLG circuits in Table-6.

Table-6

Gate/Device	elements	Delay	SwitchingEnergy
inverter	9 elements	0.022|ln(P_{error}) | ns	10.40 meV
2-input NOR	6 elements	0.060|ln(P_{error})| ns	10.70 meV
2-input OR	6 elements	0.062|ln(P_{error})| ns	10.80 meV
2-input NAND	6 elements	0.062|ln(P_{error}) |ns	10.80 meV
2-input AND	6 elements	0.062|ln(P_{error}) |ns	10.80 meV
3-input AND	7 elements	0.072|ln(P_{error}) | ns	11.58 meV
3-input NAND	7 elements	0.072|ln(P_{error}) | ns	11.58 meV
2-input XOR	13 elements	0.080|ln(P_{error})| ns	21.20 meV
3-input OR	7 elements	0.073|ln(P_{error}) | ns	11.58 meV
3-input NOR	7 elements	0.072|ln(P_{error}) | ns	11.57 meV
4-input OR	8 elements	0.078|ln(P_{error}) | ns	14.22 meV
4:1 MUX	54 elements	0.172|ln(P_{error}) | ns	103.4 meV
4-bit shifter	162 elements	0.172|ln(P_{error}) | ns	288.9 meV

We have drawn curves in reference the switching delay vs. switching error probability in Fig. 8(a) and the switching delay vs. the unit capacitance C in Fig. 8(b).

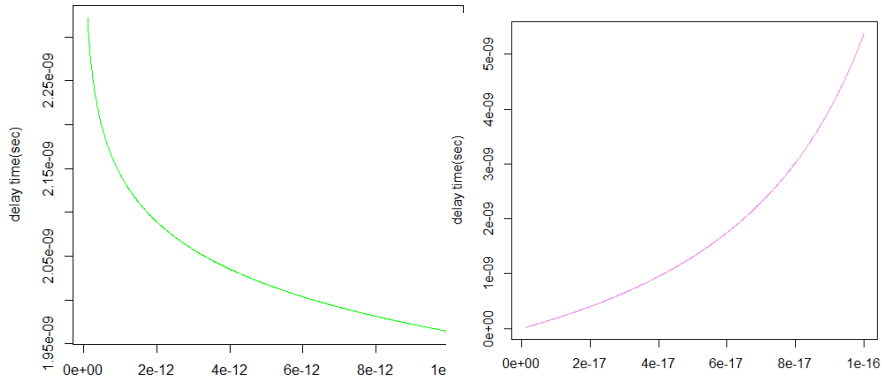


Fig. 8(a) Delay vs. Error Probability Fig. 8(b) Delay Vs. capacitance

The total number of elements required to make a gate or circuit is measured / counted. We have kept track of the data collected from this work with regard to element numbers, delays, and switching energy and they are given in Table-6.

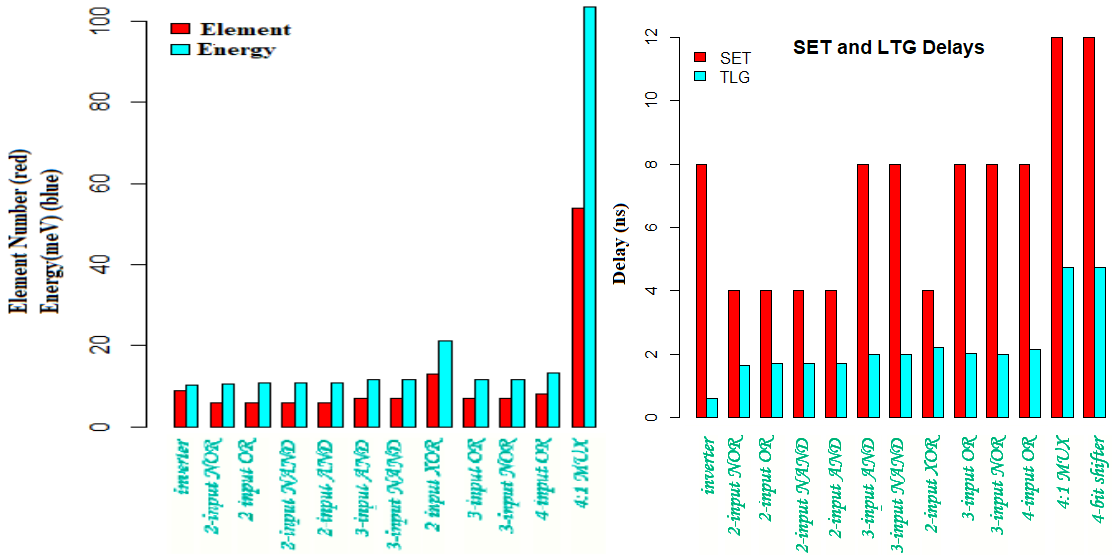


Fig. 9 comparison of Elements and switching energyFig. 10 Bar diagram of delays of SET/TLG Vs. gates

The execution delays of distinct threshold logic circuits must be different. For instance, in case of a 3-input OR gate, the processing delay is 0.073|ln(P_{error}) | ns, for 2-input XOR gate it becomes 0.080|ln(P_{error})| ns, and in the 4-bit combinational-logic shiftercircuit– delay is 0.172|ln(P_{error}) | ns.

Given the value of P_{error} = 10^{-12}, so the time after which the first output of the 4-bit combinational-logic shiftercircuit will fan out is 0.172|ln($\boldsymbol{P_{error}}$) | ns =4.75 ns. Hence, we must maintain the control signal timei.e., after every 4.75 ns or more we are to apply the control signals (C_1C_0). In this condition, the speed or frequency of the 4-bit combinational-logic shiftercircuit will be $1/4.75\ ns$ = 210.52 MHz.

When anybody is interested in finding out the circuit delays relating to CMOS, SET-based and LTG-based. The processing delaysin case of a CMOS logic gate like AND, NAND, NOR, XOR is 12ns [1-4, 8, 9]. The tunneling time through a single electron transistor (SET) [9, 10] is approximately 4ns [4-6, 12, and 13].

Table-7

Gate/Device	SET-based delay ns	LTG-based delay	Speed-up
inverter	8	0.60 ns	13.33 times
2-input NOR	4	1.65 ns	2.42 times
2-input OR	4	1.71 ns	2.33 times
2-input NAND	4	1.71 ns	2.33 times
2-input AND	4	1.71 ns	2.33 times
3-input AND	8	1.98 ns	4.04 times
3-input NAND	8	1.98 ns	4.04 times
2-input XOR	4	2.21 ns	1.81 times
3-input OR	8	2.01 ns	3.98 times
3-input NOR	8	1.99 ns	4.02 times
4-input OR	8	2.15ns	3.72 times
4:1 MUX	12	4.75 ns	2.52 times
4-bit shifter	12	4.75 ns	2.52 times

7.1 Switching delays of SET and LTG

Given that the error probability is 10^{-12} , the delays for different gates/circuits we have measured are shown in Table-7. From the Table-7, it is seen that the LTG based circuit is at least 2 times faster than the SET based circuit. And with respect to CMOS the LTG based circuit is at least 8 times faster. The delays for SET and LTG gate based circuits are represented by a bar diagram in Fig. 10.

VIII. Conclusion

Using Flip-flops, registers and memory of a computer system are made up of. Registers can be the type of right-shift or left-shift. They are all sequential circuits. By using the combinational circuit, a right-shifter or a left shifter can be implemented as we have done in this work—a 4-bit combinational-logic shifter. For implementing the shifter, multi-input-, single output- single node linear threshold logic gates are used. We have analyzed the circuit with respect to how many elements being required, processing delays, power consumption, and speed up for different circuits. Regarding combinational-logic shifter, we have simulated the circuit and the simulated result we obtained coincides with the theoretical aspects. The simulation is performed by the simulator—SIMON. Comparing to the switching delays of CMOS based circuits and SET based circuit, the TLG-based circuit is at least 8-times and 2-times faster than them respectively. The drawback of this emerging technology is that the temperature during the execution must be maintained at $0K$. In the work, control line signals must be changed after 4.75ns or more otherwise proper result will not be gained.

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