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Performance Evaluation of 21-level Reduced Switch Multi-level Inverterwith Phase Disposition and Phase Shift PWMTechniques

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Abstract
The aim of this paper is to analyze and evaluate the performance of the 21-level reduced switch multi-level inverter using phase disposition(PD) and phase shift(PS)pulse width modulation(PWM) control techniques.In this paper, a single phase 3kw, 230volt 21-level reduced switch multi-level inverterhas been designed for residential applications and its performance parameters like Total Harmonic Distortion(THD), total power losses and efficiency are discussed for both the control techniques mentioned above. This reduced switch Multi-level Inverter topology requires 24 switches to produce 21-level output voltage. The simulation of21-level Reduced Switch Multi-level Inverter with both Phase Disposition(PD) and Phase Shift(PS) PWM control Techniques has been done on MATLAB/SIMULINK.

Keywords: *Multi-level inverter(MLI), Topology, Total Harmonic Distortion(THD), Pulse Width Modulation(PWM), MATLAB/SIMULINK*

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I. INTRODUCTION

The inverter is a power electronics device which converts DC quantity into AC. The conventional two level inverters are having highly distorted output voltage waveform hence they need filters to produce smooth sinusoidal waveform as output. This makes them costly and bulkier in size and they are limited to low voltage applications as they require high voltage rated switches for high voltage applications. In order to overcome these disadvantages Multi-level inverter(MLI) concept was introduced in 1975. The Multi-level Inverters produces output voltage waveform which is almost a sinusoidal in nature. These Multi-level Inverters can be used in STATCOMs, FACTS, Active power filters, Renewable Energy Integrations, Variable Speed Drives, HVDC applications etc. The Multi-level inverters can be easily interfaced with renewable energy sources for various high power applications. There are mainly 3 types of Multi-level inverters and those are:

1. Cascaded H-Bridge(CHB) MLI
2. Flying Capacitor(FC) MLI
3. Neutral Point Clamped(NPC) MLI

Among three classical multi-level inverters, Cascaded H-Bridge MLI become a more popular because of its many advantages like it requires less no of components compared to other types, highly modular in nature, hasredundancy in switching combinationsand has fault tolerant ability. Nowadays,many researches have been going on different topologies of MLI to reduce thenumber of components requirement in making Multi-level Inverters. In the same effort, in this paper a 21-level Reduced Switch MLI topology has been introduced[2-3]. This Reduced Switch MLI is derived from conventional Cascaded H-Bridge(CHB) MLI. So, it includes all the advantages of CHB-MLI and in additionally it will reduce the number of components required, in turn which will reduce size and cost of Multi-level Inverter.In MLI, to control the operations of switches a control technique plays vital role. Choosing a promising control technique for a MLI is very much important as performance of MLI depends on control technique. After going through literature survey among multi-carrier PWM control techniques, Phase Disposition(PD) and Phase Shift(PS) PWM[3-4]control techniques have been chosen for the further study to analyze the performance parameters of 21-level reduced switch multi-level inverter and also performance evaluation of both control techniques has been doneby comparativestudy based on simulation results[5-8]. The proposed Multi-level inverter topology uses less number of power electronics components and implementation of both the control techniques is simple in circuitry. So, the inverter will be robust in structure, less costly, compact in size and can be used for low and high voltage applications.

II. TOPOLOGY AND CONTROL TECHNIQUES

The figure 2(a) shows the general diagram of the reduced switch multi-level inverter topology. Each half bridge, consists of two switches and a DC source which is called a cell. The reduced switch Multi-level Inverter topology uses 10 half bridges and one full bridge. Each half bridges, consists of two switches which are complementary in operation. In this topology, half bridges are cascaded to get higher output voltage levels and one H-bridge is connected in parallel to the cascaded half bridges to alter the polarity of the output voltage.The main drawback of Cascaded H-Bridge or reduced switch MLI is it requires isolated DC sources which limits its applications. But, this can be overcome by using Photo Voltaic cells, batteries and fuel cells as DC sources for DC power supply to the inverter.The several voltage sources on the DC side of the converter makes multilevel inverter technology a gorgeous for photovoltaic applications.

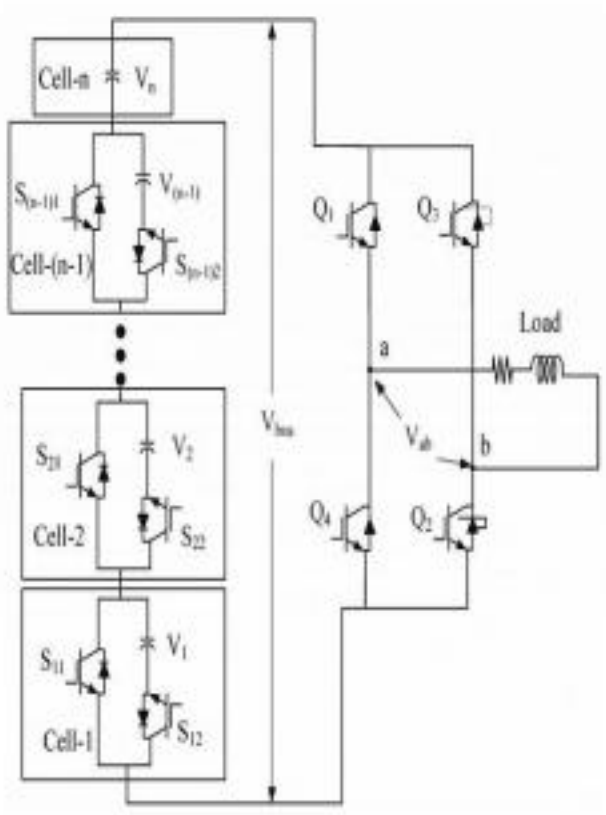


Figure 2(a) General diagram of reduced switch multi-level inverter topology

All the half bridges are connected in series to get higher output voltage levels. This topology uses 24 switches, 10 DC sources to produce 21-level output voltage. In figure 2(a), a DC source V1=Vdc and switches S11, S12 constitutes cell-1 and switches S21, S22 and a DC source V2=Vdc will constitutes cell-2 and cell-3 will be having switches S31, S32 and a DC source V3=Vdc and so on. At last the 10^{th} cell will consists of switches S101, S102 and a DC source V10=Vdc. Switches Q1, Q2, Q3, Q4 constitutes a H-bridge connected in parallel to the cascaded half bridges.

The table 2(a) shows the number of power electronics components required for all three classical multi-level inverters and Reduced Switch Multi-levelInverter(MLI). Where m is the number of output voltage levels. The number of components are calculated for m=21. The table 2(b) shows the switching states and output voltages of 21-level reduced switch multi-level inverter.At each instant, 12 switches will be in conduction. If lesser the number of conducting devices then there will be less power losses and increased efficiency.

COMPONENTS	Neutral Point Clamped(NPC) MLI	Flying Capacitor(FC) MLI	Cascaded H-Bridge(CHB) MLI	Reduced Switch MLI
Main Switching devices	2(m-1)=40	2(m-1)=40	2(m-1)=40	(m-1)+4=24
Anti-parallel diodes	2(m-1)=40	2(m-1)=40	2(m-1)=40	(m-1)+4=24
Clamping diodes	(m-1)(m-2) =380	0	0	0

DC bus capacitors	(m-1)=20	(m-1)=20	(m-1)/2=10	(m-1)/2=10
Flying capacitors	0	(m-1)(m-2)/2 =190	0	0

Table 2(a)the number of power electronics components required in different MLI topologies

Sl No.	Switches turned ON	Output voltage
1	S12,S22,S32,S42,S52,S62,S72, S82,S92,S102,Q1,Q2	+10Vdc
2	S12,S22,S32,S42,S52,S62,S72, S82,S92,S102,Q3,Q4	-10Vdc
3	S12,S22,S32,S42,S52,S62,S72, S82,S92,S101,Q1,Q2	+9Vdc
4	S12,S22,S32,S42,S52,S62,S72, S82,S92,S101,Q3,Q4	-9Vdc
5	S12,S22,S32,S42,S52,S62,S72, S82,S91,S101,Q1,Q2	+8Vdc
6	S12,S22,S32,S42,S52,S62,S72, S82,S91,S101,Q3,Q4	-8Vdc
7	S12,S22,S32,S42,S52,S62,S72, S81,S91,S101,Q1,Q2	+7Vdc
8	S12,S22,S32,S42,S52,S62,S72, S81,S91,S101,Q3,Q4	-7Vdc
9	S12,S22,S32,S42,S52,S62,S71, S81,S91,S101,Q1,Q2	+6Vdc
10	S12,S22,S32,S42,S52,S62,S71, S81,S91,S101,Q3,Q4	-6Vdc
11	S12,S22,S32,S42,S52,S61,S71, S81,S91,S101,Q1,Q2	+5Vdc
12	S12,S22,S32,S42,S52,S61,S71, S81,S91,S101,Q3,Q4	-5Vdc
13	S12,S22,S32,S42,S51,S61,S71, S81,S91,S101,Q1,Q2	+4Vdc
14	S12,S22,S32,S42,S51,S61,S71, S81,S91,S101,Q3,Q4	-4Vdc
15	S12,S22,S32,S41,S51,S61,S71, S81,S91,S101,Q1,Q2	+3Vdc
16	S12,S22,S32,S41,S51,S61,S71, S81,S91,S101,Q3,Q4	-3Vdc
17	S12,S22,S31,S41,S51,S61,S71, S81,S91,S101,Q1,Q2	+2Vdc
18	S12,S22,S31,S41,S51,S61,S71, S81,S91,S101,Q3,Q4	-2Vdc
19	S12,S21,S31,S41,S51,S61,S71, S81,S91,S101,Q1,Q2	+Vdc
20	S12,S21,S32,S41,S51,S61,S71, S81,S91,S101,Q3,Q4	-Vdc
21	S11,S21,S31,S41,S51,S61,S71, S81,S91,S101,Q1,Q2	0

Table 2(b) switching states and output voltages of 21-level reduced switch multi-level inverter.

Phase Disposition PWM control technique is a multi-carrier PWM method where all the carrier waveforms are identicalin magnitude and frequency but, they are all vertically phase shifted or vertically shifted from one another. This PWM method uses n-1 carrier waveforms to generate gate pulses for n-level inverter and operates all the switches such that the fundamental voltage from each cell gets added up to produce higher voltage levels.

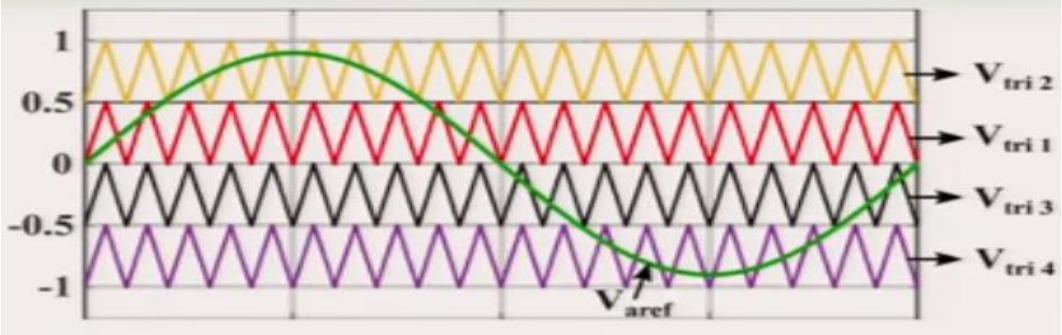
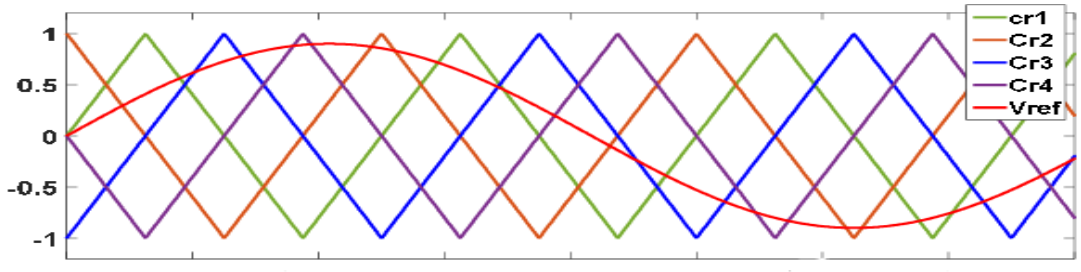


Figure 2(b)Phase Disposition PWM Waveforms

Phase Shift PWM control technique is a multi-carrier PWM method where all the carrier waveforms for each cell are identical but they are phase shifted from each other. The carrier waveforms are identical in magnitude and frequency but they are phase shifted from each other. This PWM technique will also uses n-1 carrier waveforms but these carrier waveforms will have phase shift of an angle Φ between each other. Phase shift angle Φ can be calculated as below



Φ=360/(n-1) where n is number of levels
Figure 2(c) Phase Shift PWM Waveforms

III. SIMULATION

3.1Design Aspects

A 3KW, 230V reduced switch multi-level inverter is designed for domestic applications where DC supply to inverter is fed through solar PV cells.For Resistive(R) load, output active power Po can calculated as $Po=V_{orms}*I_{Lrms}$where V_{orms} is RMS values of output voltage and$I_{Lrms}$is RMS value of the load current.Po=3000W V_{orms}= 230V then $I_{Lrms}=Po/V_{orms}=3000/230=13.04A$ At full load, $I_{Lrms}=13.04A$ then load Resistance $R=V_{orms}/I_{Lrms}=230/13.04=17.64Ohm$. For Resistive-Inductive (RL) load, let's consider induction motor as load and its load power factor(PF) as 0.8 then output power Po can calculated as $Po=V_{orms}*I_{Lrms}*PF$where V_{orms} is RMS values of output voltage and $I_{Lrms}$is RMS value of the load current. Po=3000W V_{orms}= 230V then $I_{Lrms}=Po/(V_{orms}*PF)=3000/(230*0.8)=16.3A$.At full load, $I_{Lrms}=16.3A$ then load Impedance $Z=V_{orms}/I_{Lrms}=230/16.3=14.11Ohm$.We know that PF=R/Z therefore the load resistance $R=PF*Z=0.8*14.11=11.29Ohm$, inductive reactanceis $X_L = \sqrt{(Z*Z - R*R)}= \sqrt{(14.11*14.11 - 11.29*11.29)}=8.46ohm$, the load inductance L can be calculated as $L=X_L/(2*3.142*f)$ wher f is the frequency=50Hz. L=8.46/(2*3.142*50)=26.94mH.

3.2 Specifications

The table 3.2 shows the various parameters and their values involved in simulation of 21-Level reduced switch Multi-Level Inverter with Phase Disposition and Phase Shift PWM control techniques.

Parameters	Values
Supply Voltage Vdc	33V
Reference waveform peak to peak voltage Vref(p-p)	20V
Carrier waveform peak to peak Voltage Vc(p-p)	PDPWM- 1V PSPWM-20V
Reference waveform frequency Fr	50Hz
Carrier waveform frequency Fc	1000Hz
ON State Resistance Ron of MOSFET	0.039ohm
ON State Resistance Ron of Diode	0.01ohm

Table 3.2 Specifications

3.3 Simulink modeling of Phase Disposition PWM technique

The figure 3.3 shows the implementation of Phase Disposition PWM technique on SIMULINK for the one cell. The Vc1 will have magnitude [0 1 0] at instants of [0 0.5 1] milliseconds that means, at time t=0 the magnitude of Vc1 will be zero and at t=0.5millisec the magnitude of Vc1 is 1 and again at t=1ms magnitude become zero. Similarly carrier Vc2 will havemagnitude of -1 at t=0, 0 at t=0.5ms and -1 at t=1ms. Then amplitude of Vc1and Vc2 are compared with sinusoidal reference waveform Vref using relational operators. Then by usinglogical operators exclusive-OR and NOT, the switching pulses for two switches are generated.The logicalImplementation can be interpreted as, if carrier waveform Vc1 is greater than reference waveform Vref or if carrier waveform Vc2 is less than reference waveform Vrefthen only turn ON the switch S1 otherwise turn ON the switch S2. In the same way, the switching pulses are generated for the other cells.

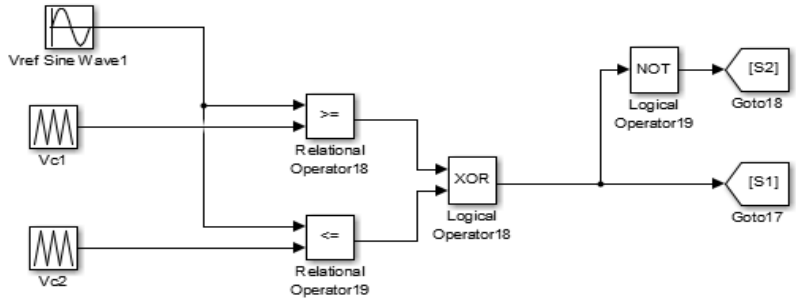


Figure 3.3 the logical implementation of Phase Disposition PWM technique for cell-1

3.4 Simulink modeling of Phase Shift PWM technique

The figure 3.4 shows the implementation of Phase Shift PWM technique on SIMULINK for the one cell.

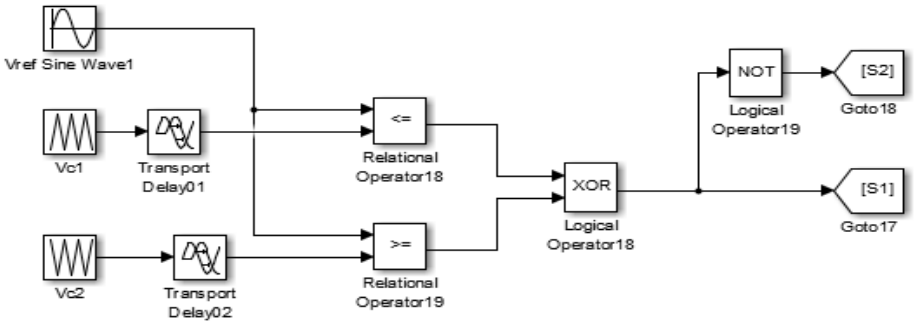


Figure 3.4 the logical implementation of Phase Shift PWM technique for cell-1

The Vc1 will have magnitude [-10 0 10 0 -10] at instances of [0 0.25 0.5 0.75 1] milliseconds. That means, the magnitude of Vc1 will be -10 at time t=0, 0 at t=0.25ms, 10 at t=0.5ms, 0 at t=0.75 and -10 at t=1ms. Carrier Vc2 should have phase delay of 180degree with respect to Vc1 but this phase delay can be achieved by giving amplitude values as [10 0 -10 0 10] at the instances of [0 0.25 0.5 0.75 1]ms.Then amplitude of Vc1and Vc2 are compared with sinusoidal reference waveform Vref using relational operators. Then by using logical operators exclusive-OR and NOT, the switching pulses for two switches are generated. From figure 3.4, the logical implementation can be interpreted as, if carrier waveform Vc1 is less than reference waveform Vref or if carrier waveform Vc2 is greater than reference waveform Vref then only turn ON the switch S1 otherwise turn ON the switch S2. In the same way, the switching pulses are generated for the other cells.

IV. RESULT DISCUSSION

4.1 Simulation Results of 21-level reduced switch MLI with Phase Disposition PWM control technique The figure 4.1(a), (b), (e) and (f) shows the output voltage and load current waveforms of 21-level reduced switch Multi-level Inverter onResistive(R) and Resistive-Inductive (RL) Load. The figure 4.1(c), (d), (g) and (h) shows the Total Harmonic Distortion(THD) in output voltage and load current waveforms. The output voltage waveform will have 21 voltage levels as shown in switching table 2(b). In RL load, the load inductor L acts a filter for current hence load current waveform become pure sinusoidal in nature.

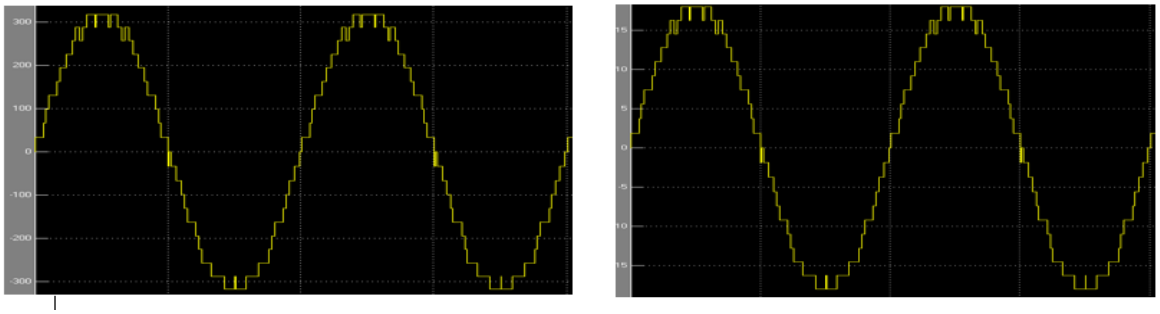


Figure 4.1(a) output voltage waveform and (b) Load current waveform

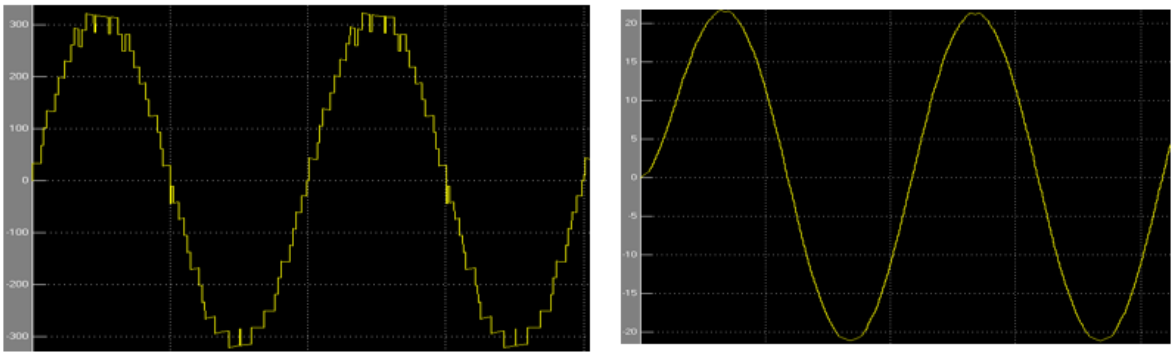


Figure 4.1 (c) Voltage waveform THD(%) and (d) Current waveform THD(%)

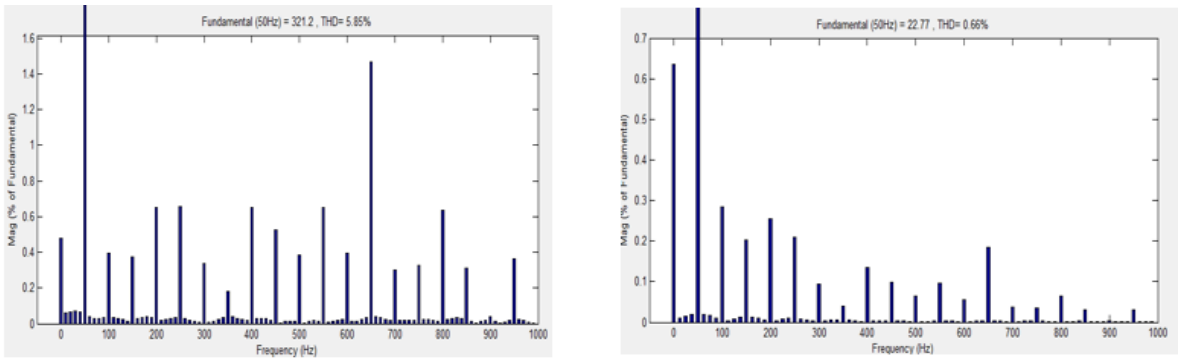


Figure 4.1(e) output voltage waveform and (f) Load current waveform

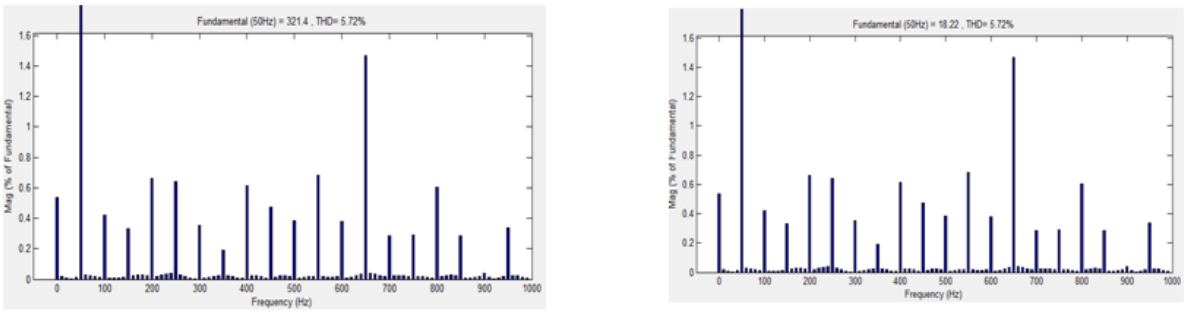


Figure 4.1 (g) Voltage waveform THD (%) and (h) Current waveform THD(%)

For analysis of THD and efficiency of reduced switch muli-level inverter, different loadings have been considered.The table 4.1(a) shows the simulation results of 21-level Reduced Switch-MLI with pure Resistive(R) load and Table 4.1(b) shows the simulation results of 21-level Reduced Switch-MLI with pure Resistive-Inductive (RL) load. Where, $I_{o(calc)(}$is calculated RMS value of load current and Iorms is measured RMS values of load current.

Loading	Load Current $I_{o(calc)(}$A)	Load Resistance R(ohm)	Output voltage (Volt)	Iorms (A)	THD (%)	Supply Power (W)	Output power (W)	Power Loss (W)	Efficiency (%)
Full load(FL)	13.04	17.64	227.7	12.91	5.72	2970	2930	40	98.65
¾ th of FL	9.78	23.52	229.3	9.749	5.743	2256	2228	28	98.75
Half load	6.52	35.28	230.9	6.545	5.75	1521	1506	15	99.01
Quarter load	3.26	70.55	232.6	3.296	5.758	769.9	764	5.9	99.23
No Load	0	-	234.2	0	5.767	0	0	-	-

Table 4.1(a) simulation results of 21-level RS-MLI with R load

Loading	Load Current $I_{o(calc)}$ (A)	Load Resistance R(ohm)	Load Inductance L (mH)	Output voltage (Volt)	I_{orms} (A)	Volt. THD (%)	Curr. THD (%)	Supply Power (W)	Output power (W)	Losses (W)	Efficie-ncy (%)
Full load(FL)	16.3	11.29	26.94	227.7	16.11	5.85	0.808	2976	2930	46	98.45
¾ th of FL	12.22	15.05	35.9	229.3	12.17	5.835	0.798	2255	2229	26	98.85
Half load	8.15	22.57	53.78	230.9	8.177	5.81	0.791	1521	1509	12	99.21
Quarter load	4.07	45.2	107.9	232.6	4.109	5.787	0.787	766.5	763.3	3.2	99.58
No Load	0	-	-	234.2	0	5.767	-	-	-	-	-

Table 4.1(b) simulation results of 21-level RS-MLI with RL load

The voltage regulation of the Multi-Level Inverter can be found by formula $((V_{no_load} - V_{full_load})/V_{full_load})*100$and that is ((234.2-227.7)/227.7)*100 =2.85%.The 21-level reduced switch multi-level inverter with phase disposition PWMcontrol technique at full load has efficiency of 98.65% for R load and 98.45% for RL load. As per IEEE std 519-2014 the THD at any common coupling point(PCC) in a power system has to be within 8% for operational rated voltage less than 1kv. This inverter has maximum Total Harmonic Distortion(THD) of 5.85% which is within the IEEE standards. As the loading decreases from full load to no load, the THD varies in decimal places for both R and RL loads.

4.2 Simulation Results of 21-level reduced switch MLI with Phase Shift PWM control technique The figure 4.2 (a), (b), (e) and (f) shows the output voltage and load current waveforms of 21-level reduced switch Multi-level Inverter on Resistive(R) and Resistive-Inductive (RL) Load. The figure 4.2(c), (d), (g) and (h) shows the Total Harmonic Distortion(THD) in output voltage and load current waveforms. The output voltage waveform will have 21 voltage levels as shown in switching table 2.4(b).

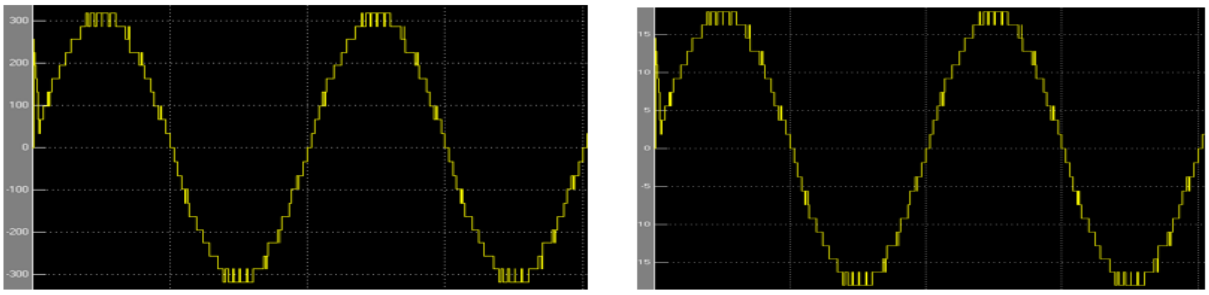


Figure 4.2(a) output voltage waveform and (b) Load current waveform

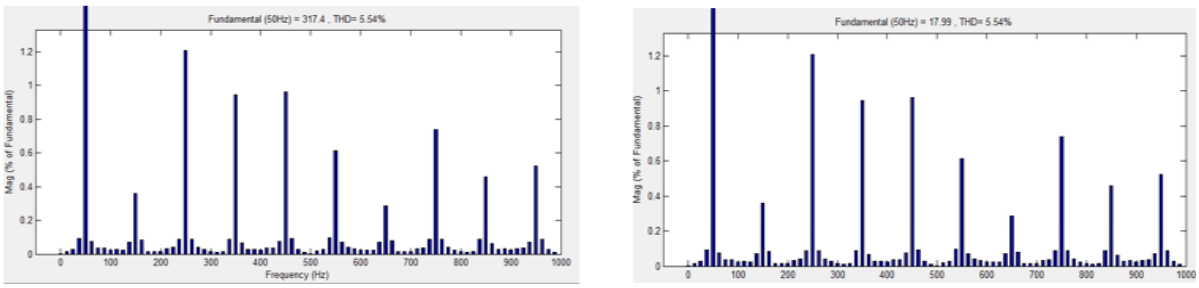


Figure 4.2 (c) Voltage waveform THD(%) and (d) Current waveform THD(%)

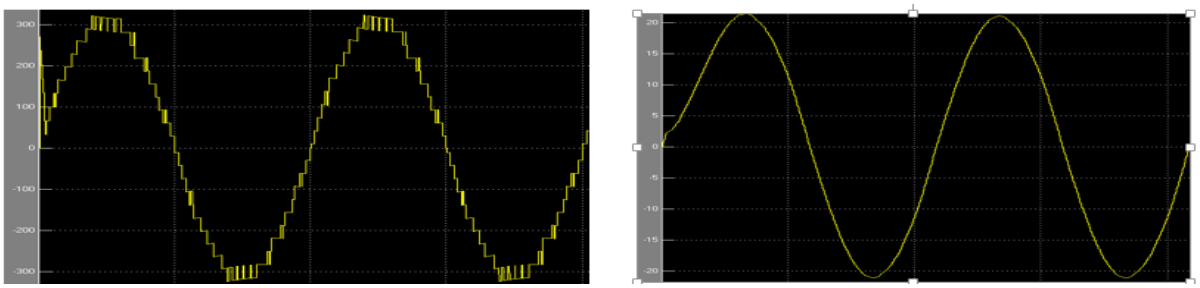


Figure 4.2(e) output voltage waveform and (f) Load current waveform

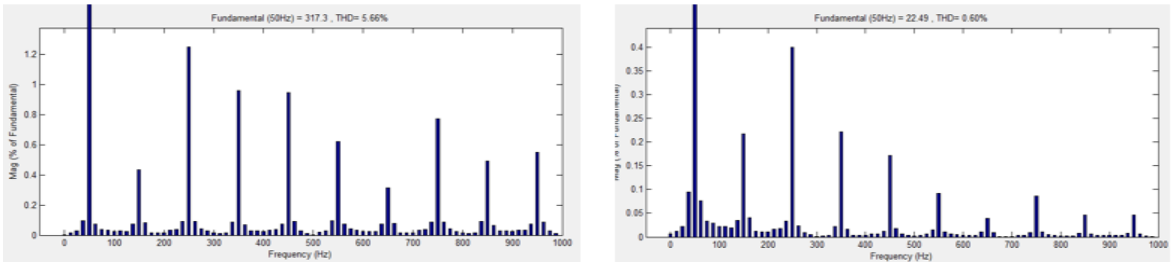


Figure 4.2 (g) Voltage waveform THD(%) and (h) Current waveform THD(%)

When MLI on RL load, the peak value of fundamental output voltage is 317.3 volt and peak value of fundamental component of the load current is 22.49A at full load. The output voltage waveform has THD of 5.66% and load current waveform has THD of 0.60%.For analysis of THD and efficiency of reduced switch muli-level inverter, different loadings have been considered.The table 4.2(a) shows the simulation results of 21-level Reduced SwitchMLI with pure Resistive(R) load and table 4.2(b) shows the simulation results of 21-level Reduced Switch-MLI with pure Resistive-Inductive (RL) load. Where, $I_{o(calc)(}$is calculated RMS value of load current and Iorms is measured RMS values of load current

Loading	Load Current $I_{ocalc)(}$A)	Load Resistance R(ohm)	Output voltage (Volt)	Iorms (A)	THD (%)	Supply Power (W)	Output power (W)	Power Loss (W)	Efficiency (%)
Full load(FL)	13.04	17.64	224.9	12.75	5.54	2990	2860	130	95.65
¾ th of FL	9.78	23.52	226.5	9.631	5.466	2268	2175	93	95.9
Half load	6.52	35.28	228.1	6.465	5.47	1529	1470	59	96.14
Quarter load	3.26	70.55	229.7	3.256	5.475	773.8	745.6	28.2	96.36
No Load	0	-	231.3	0	5.481	0	0	-	-

Table 4.2(a) simulation results of 21-level RS-MLI with R load

Loading	Load Current $I_{o(calc)}$ (A)	Load Resistance R(ohm)	Load Inductance L (mH)	Output voltage (Volt)	I_{orms} (A)	Volt. THD (%)	Curr. THD (%)	Supply Power (W)	Output power (W)	Losses (W)	Efficiency (%)
Full load(FL)	16.3	11.29	26.94	224.9	15.92	5.66	0.60	2989	2860	129	95.68
¾ th of FL	12.22	15.05	35.9	226.5	12.02	5.55	0.699	2265	2176	89	96.07
Halfload	8.15	22.57	53.78	228.1	8.076	5.526	0.686	1527	1473	54	96.46
Quarter load	4.07	45.2	107.9	229.7	4.06	5.502	0.678	769.8	744.9	24.9	96.76
No Load	0	-	-	231.3	0	5.481	-	-	-	-	-

Table 4.2(b) simulation results of 21-level RS-MLI with RL load

The voltage regulation of the MLI can be found by formula $((V_{no_load} - V_{full_load})/V_{full_load})*100$and that is ((231.3-224.9)/224.9)*100 = 2.84%.The 21-level reduced switch multi-level inverter with phase shift PWM control technique at full load, has efficiency of 95.08% for both R and RL load. The inverter has maximum Total Harmonic Distortion(THD) of 5.763% which is within the IEEE standards.

V.CONCLUSION

Simulation of 21-level reduced switch multi-level inverter with both Phase Disposition(PD) and Phase Shift(PS) PWM control techniques has been done using MATLAB/SIMULINK and simulation results have been discussed. The 21-level reduced switch multi-level inverter at full load with Phase Disposition PWM control technique has THD of 5.85% and efficiency of 98.45% for RL load and same inverter at full load with Phase Shift PWM control technique has THD of 5.66% and efficiency of 95.68% for RL load. So, Phase Shift PWM method is superior in THD and inferior in efficiency compared to Phase Disposition PWM method. As THD for both the control techniques are within the limits of IEEE standard 519-2014, we can choose Phase Disposition PWM control technique over Phase Shift PWM technique as multi-level inverter has more efficiency with Phase Disposition PWM control technique.

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