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Two Stage Power Conversion of Photovoltaic-Ultra capacitor Configuration for efficient Operation

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Abstract
There has been a remarkable increase in the penetration of photovoltaic (PV) grid connected systems in the last decade, and this trend is bound to increase at a much faster pace in the near future. The main advantage of a grid connected PV system is its simplicity, relatively low operating and low maintenance costs as well as reduced electricity bills. But still the PV system cannot provide a constant output due to the sudden changes in solar irradiance and short term voltage dips. This work proposes an efficient Photovoltaic-Ultra capacitor configuration for enhanced operation irrespective of the changes in solar input. Utilization of an ultra-capacitor (UC)-based energy storage device can provide one of the most efficient solutions for short-term operational challenges in grid-connected photovoltaic (PV) systems. The effectiveness of the proposed method is examined by MATLAB-SIMULINK based simulations.

Keywords:*Photovoltaic Energy Generation, Ultra Capacitor, Maximum Efficiency, Super Capacitor*

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I. INTRODUCTION

As we know the importance of PV systems are increasing day by day since the photovoltaic energy generation is clean and silent. But as being an intermittent energy generation, the PV systems should be controlled effectively in order to enhance its operations. There are several methods are available for the reliable operations of photo voltaic systems. Photovoltaic systems can be broadly classified as standalone and grid-connected PV systems. In a conventional two-stage PV system, the first stage comprises of the PV panel interfaced to the DC link via a Boost Converter and the second stage comprises of a 3 − φ voltage source converter (VSC) with an LCL filter (typically).

As the penetration levels continue to increase, the PV systems are being progressively used for active regulation of voltages and power quality issues in distribution system. However, there are several challenges in the operation of PV systems integrated to distribution networks and weak grids. This work introduces an enhanced Two-stage PV system configuration utilizing ultracapacitors (UCs). As compared to transmission networks, the effect of dynamic changes in solar intensity (due to fast-moving clouds) is more pronounced in distribution systems and weak grids. Typically, in the presence of solar intensity variations, the boost converter associated with the PV plant can be controlled to extract the maximum power. .However, the control is complex and there is a net drop in the active power injected into the grid that results in undesirable variations in the voltages. One way to overcome this challenge is to utilize an energy storage device (that can compensate for the drop in active power from the PV panel) together with the PV system.

1.1. Ultra Capacitors

Ultracapacitors, or super capacitors as they are also known, are an energy storage technology that offers high power density, almost instant charging and discharging, high reliability, and very long lifetimes. Advantages of Ultracapactiors are, Long lifetimes, Maintenance-free and reliable., Near full efficiency even in extreme temperatures, from -40 °C to 65 °Cup to 60 times the power density achieved by batteries.and 30% more efficient than batteries

1.1.1 PV-Ultra capacitor System

As compared to the conventional PV system, the pro-posed configuration has an ultra-capacitor stack connected to the DC link via the bidirectional DC/DC converter. The ultra-capacitor stack is charged through

the bidirectional DC/DC converter using the power from the PV source, and the same can be discharged in scenarios where additional power is needed.

For operating conditions, such as the presence of low voltages at PCC and sudden changes in solar irradiation (due to fast moving clouds), the energy storage device must be capable of supporting the PV system by providing higher values of power at a very short time (i.e., higher power density . Hence, as compared to PV-battery configuration, a PV-UC configuration (as shown in Fig.1.) is a more efficient solution for handling fast moving clouds and temporary low voltages at the PCC.

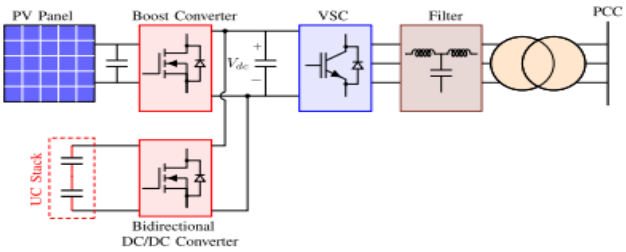


Figure 1: Block diagram of proposed Configuration

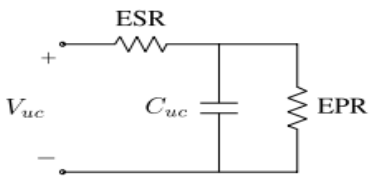
The steps involved in designing a PV-ULTRACAPACITOR SYSTEM include:
(a) Modeling of the PV system, ,(b) Modeling and control of boost converter (connecting the PV panel to the DC link),(c) Modeling and control of the 3 − φ inverter,(d) Modeling of the ultracapacitor and (e) Modeling and control of the bidirectional DC/DC converter

1.2 FRAME WORK OF PV-UC SYSTEM

The design of this system includes (a) The modeling and multi-mode operation of the ultra capacitor along the associated DC/DC converter, (b) Control of UC based bidirectional DC/DC converter (c) Coordination of the 3 − φ VSC and the bidirectional DC/DC converter (associated with UC) under low voltages and sudden changes in solar irradiance.

1.2.1Modeling and Sizing ofUltra capacitor Stack

An ultra-capacitor can be represented by various equivalent circuit models that capture its terminal behavior (charging, discharging and open circuit) to various levels of accuracy.



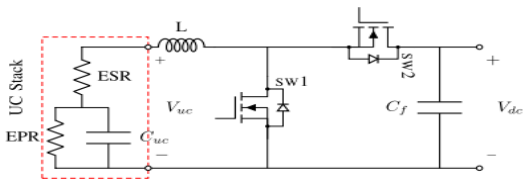


Figure 2: Equivalent circuit of Ultra capacitorFigure 3: Bidirectional Dc to DC converter

This model comprises of a simple RC circuit with two resistors. The resistance in parallel to the capacitor is referred to as equivalent parallel resistance (EPR), and one in series is referred to as equivalent series resistance (ESR). The EPR represents the self-discharge phenomena of the ultra-capacitor under no-load operation (idle state). Typically, there is a sudden drop in the voltage at the end of the charging cycle and the sudden rise in the voltage at the end of the discharging cycle due to the ESRF or practical applications, the individual UC cells are usually stacked together (referred to as UC stack) and interface to the DC link via the bidirectional DC/DC converter

1.2.2 Bidirectional Dc to DC converter

The typical configuration of a bidirectional DC/DC converter used to interface the UC stack with the PV-system is shown in Fig.3.1.2. The filter inductor (L) of the bidirectional DC/DC converter is designed based on the maximum allowable current ripple (δi; expressed as a fraction of average current. Depending on the network operating condition and the solar irradiance, the bidirectional DC/DC converter can operate in at most 3 different modes. 1) Mode 1 - Charging cycle: During the charging cycle (SW1 is OFF and SW2 is controlled using pulse width modulation (PWM)), the UC stack gets charged via the DC link, and the converter acts as a buck converter. 2) Mode 2 - Discharging cycle: During the discharge cycle (SW1 is controlled using PWM and SW2 is OFF), the UC stack acts as an additional source with the converter behaving like a boost converter. 3)

Mode 3 - PWM blocking: In this mode, the converter is in Idle state with both the switches (SW1 and SW2) being in OFF state

1.2.3 Coordinated control of 3 − φ vs. and uc stack

An algorithm to coordinate the 3 − φ inverter and the UC stack in the presence of low voltages at PCC is presented. Apart from determining the charging (C) and discharging (D) signal, the coordination methodology also determines the reference values to be given as an input to the controller associated with the UC stack.

The reference values to the 3 − φ VSC under low voltages are the currents i ∗ d and i ∗ q and hence the control architecture comprises of only current control. The controllers employed in current control are the PI controllers, whose tuning depends on the plant transfer function (G(s); which is determined by the filter). Although this work employs an LCL filter, for the purpose of controller design, the parameters of the PI controller can be tuned by assuming that it to be an equivalent inductive filter i.e. Lt = L1 + L2.

1.2.4 Control of Bidirectional Dc/Dc Converter (UC stack)

There are two conditions at which the ultra-capacitors can work for the photo voltaic system. They are mentioned are when there is a sudden change in the irradiance (such as cloud passage), the output power (*Ppv*) from the PV panel is reduced and in order to keep the DC link voltage at the desired value, the inverter has to process a reduced amount of power (in the absence of UC stack). This temporary reduction in power processed by the inverter (which is the amount of power injected into the grid) is undesirable and can be avoided if the UC stack is controlled to provide the miss- match between the inverter set point (i.e., *Pinv* and *Qinv*) and the power produced by the PV panel. Hence during sudden changes in irradiance, the *D* signal of the UC stack must be toggled high, and the UC stack must be controlled to track the power that is the difference between *Pinv* and *Ppv* **.Presence of low voltages at pcc (LVRT)**. In the event of low voltage at the PCC, the PV system must stay connected to the grid for a minimum duration of time and must provide some reactive power support. The ride through duration (*Tr*) and reactive support requirements as per in shown in Figure.Where (*vgd*, *vqg*) and (*id*, *iq*) represent the components of grid voltage and grid current (i.e. towards the grid side inductor of LCL _filter) in rotating reference frame (RRF), respectively.Typically, the *d*axis of the RRF is oriented along the grid voltage using PLL, and as a result, *vgd* D *Vg*, *vqg* D0

II. MAXIMUM POWER POINT TRACKING

Incremental conductance is an electronic technique to operate the PV system at its maximum power point.

- It Improves the efficiency of solar pan rapidly changing atmospheric conditions

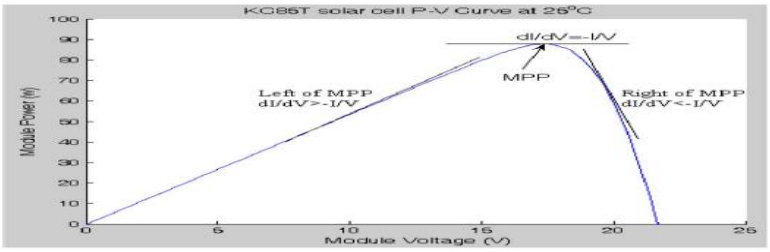


Figure 4: MPPT curve

The incremental conductance algorithm detects the slope of the P–V curve, and the MPP is tracked by searching the peak of the P–V curve. This algorithm uses the instantaneous conductance I/V and the incremental conductance dI/dV for MPPT. An MPPT, or maximum power point tracker is an electronic DC to DC converter that optimizes the match between the solar array (PV panels), and the battery bank or utility grid. The incremental conductance algorithm detects the slope of the P–V curve, and the MPP is tracked by searching the peak of the P–V curve. ... In the conventional incremental conductance algorithm, (8) is used to detect the MPP, and the voltage and current of the PV module are measured by the MPPT controller

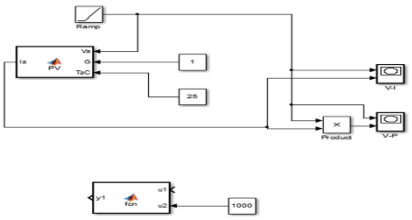
III. RESULT AND DISCUSSION

3 SIMULATION

The performance of the proposed approach is analysed using MATLAB simulations. In order to emulate a weak grid scenario, the grid resistance and inductance are chosen as 0:1Ω and 4:5 mH, respectively. The rest of the system data is chosen as shown in section 5.2.In the case of weak grids, such dips can happen even due to a sudden increase in loads. In the final case study, the performance of the proposed algorithm in the

presence of voltage dips of severe magnitude is analyzed. For this purpose, a 3 − φ fault with a fault impedance of zf = 4 Ω is created at the PCC of PV system 1.

The simulation diagram of the PV system along with an ultracapacitor is shown below. Here a sine wave of 1000 amplitude is given as the irradiance and temperature is given as a constant say 25



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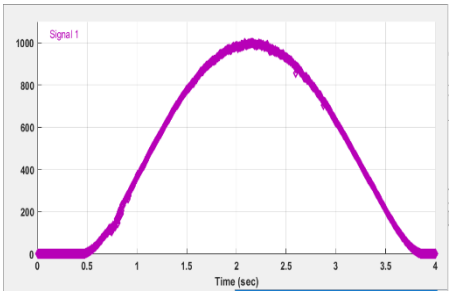


Figure 5: MATLAB modeling of PV moduleFigure 6:Irradiance signal

3.2 Modelling Of the Block Diagram

The modelling of the block diagram is done in the MATLAB and the step by step procedures are as follows:To a PV array , a constant sin wave of irradiance equal to (1000wb/m^2)is given (shown in the figure figure:4.3.1.1)and the value of tempature constant is selected as 25

- Then the output of the Pv panel is connected to a boost converter. The function of the boost converter is to increase the voltage level to a higher value and the value of the resister is selected as (1e-4) and the capacitance as (100e-6).In the output section of the boost converter, an IGBT and a diode is connected in series and it makes a shunt connection with a capacitor. The value of snubber resistance is 500 ohms and the snubber capacitance is (250e-9) farad. Snubber circuits are essential for diodes used in switching circuits. It can save a diode from overvoltage spikes, which may arise during the reverse recovery process. A very common snubber circuit for a power diode consists of a capacitor and a resistor connected in parallel with the diode
- The output of the boost converter will give dc bus voltage and a voltage measurement block is connected across it. At the same time the Ultra capacitor is connected across the dc bus. Ultracapacitor is a combination of several capacitors either in series or in parallel.A **supercapacitor** (**SC**), also called an **ultracapacitor**, is a high-capacity capacitor with a capacitance value much higher than other capacitors, but with lower voltage limits, that bridges the gap between electrolytic capacitors and rechargeable batteries. It typically stores 10 to 100 times more energy per unit volume or mass than electrolytic capacitors, can accept and deliver charge much faster than batteries, and tolerates many more charge and discharge cycles than rechargeable batteries.
- Since a capacitor blocks dc voltage and hence we cannot connect a ultra capacitor with dc bus .So we need to design an equivalent circuit of Ultra capacitor stack in which one resistance is connected in series with UC (ESR) and other one is connected in parallel with UC (EPR).The value of ESR is taken as 100 ohms and EPR is 50 ohms. Up to this point dc side will be ready and now we have to model the ac side.The sizing of the ultracapacitor stack depends on (a) the desired power level (i.e., the power level required as a backup for the PV system), (b) the typical duration of discharge and (c) the minimum allowable discharge voltage of the ultracapacitor stack. Given the discharge power (P0), duration of discharge (1t) and rated voltage across the UC stack (Vuc,n),The output from the UC stack is then given to the input side of three phase voltage source inverter .The values of snubber resistance is selected as according to the design. The voltage and current measurement can be done by using voltage measurement loops. After the conversion of dc to ac, it is given to a filter in order to reduce the ripples.To both converter and inverter, pwm pulses are required and pwm generators are implemented in the design section

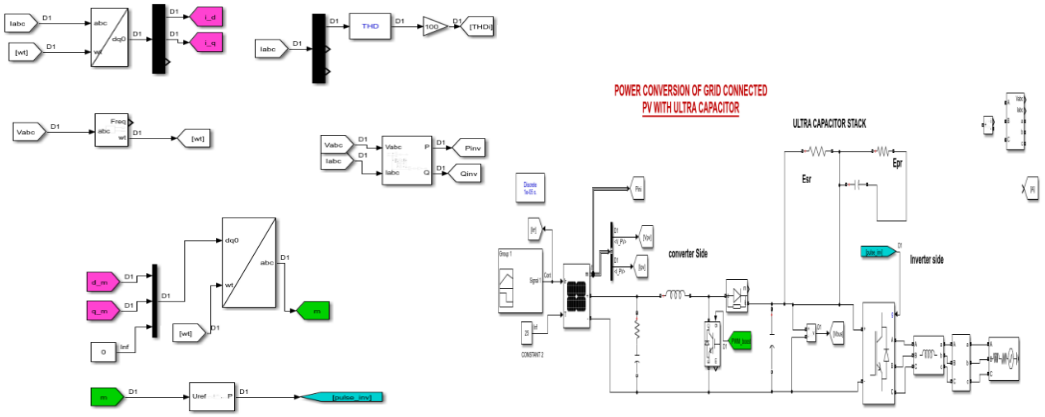
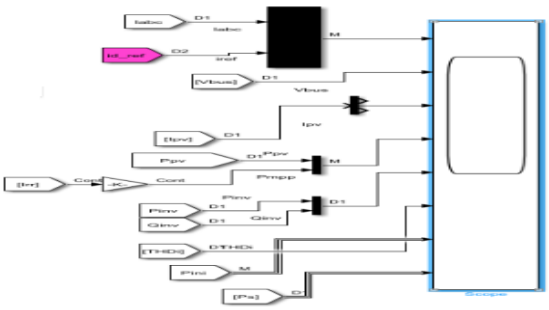


Figure 7: MATLAB modeling of Block diagramFigure 8: Controlling Schemes

3.3 Implementation of Controlling Circuits in to the System

A well working control system is needed for the efficient working of the overall system. There are three PI(Proportional & Integral) controllers are needed.The first controller is needed for the proper biasing of the dc bus voltage. In order to get a ripple free output at the ac side, the dc bus voltage should be constant. A reference voltage of 800 v is taken and it is made to compare with the dc bus voltage. Whenever the dc bus voltage is less than the reference value, the controller will set the reference value as the output and it will be given as an input signal to the inverter. The second PI controller is needed for comparing the two currents id and id ref of the dc bus voltage and the last controller controls the iq component. All the three PI controllers are connected with the saturation block.The output waveforms can be studied with the help of a scope.Here 8 inputs are given to the scope and different output waveforms are verified.



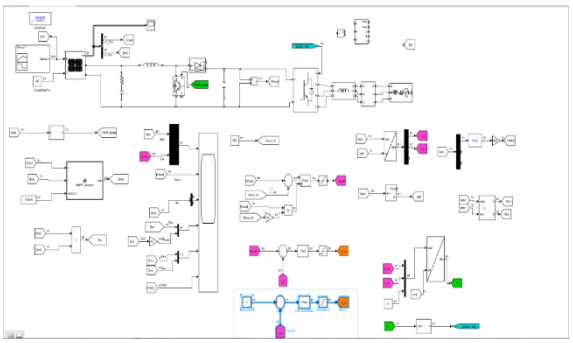


Figure 9: Inputs connected to the scope Figure 10: Overall system model in MATLAB

IV. SIMULATION ALGORITHM

The simulation algorithm for the simulation of converter and inverter is given below.The values assigned to the different variables are given in the table 4.4.2.1

```
Ts = 10e-6;     % sampling time
P = 50e3;       %Rated power
U = 380;        % inverter phase2phase voltage
f = 50;         % grid frequency
fsw = 5e-3;     %switching frequency of inverter
Lf=((0.1*U^2)/(2*pi*f*(p/3)));%design of boost converter
Vmpp = 406;
V_bus_ref = 800;
Vin = Vmpp;   %input voltage of boost converter
Vo = V_bus_ref; %output voltage of boost converter
fsw_boost = 5e3; %switching frequency of boost converter
D = 1-(Vin/Vo);
L bound = ((1-D)^2)*D*(Vo^2)/(2*fsw boost*p);
L_boost = 10*L_bound;
C_boost_min = (D*P)/(0.01*Vo^2*fsw_boost);
C_boost = 1000e-6;
```

V. SIMULATION RESULTS

The performance of the proposed algorithm is presented for a scenario where there is a sudden change in solar irradiation due to cloud passage. The solar irradiance is presumed to fall to 50%, and the duration of this fall is presumed to be around 4:5 s (within the typical duration range reported . The output power from the PV panel during this period (dip starting at 0:3 s) is shown in Fig.11.In the absence of UC stack, the power processed by the 3 − φ VSC is same as that of the PV power (as shown in Fig.13 and with the grid being weak, this sudden dip in irradiance causes the voltage at PCC to drop below 0.95 p.u. (as shown in Fig. 14 As shown in Fig 15, for the operating condition under study, the UC stack is pumping the additional power which is the mismatch between the inverter set point and the power output from PV array. The additional power injected by the UC stack can help in improving the voltage at PCC as shown in Fig.13.On the other hand, by utilizing an UC based energy storage and controlling it by using the proposed algorithm, the power reduction due to dip in irradiance can be compensated using the UC stack. As shown in Fig.15, for the operating condition under study, the UC stack is pumping the additional power which is the mismatch between the inverter set point and the power output from PV array. The additional power injected by the UC stack can help in improving the voltage at PCC as shown in Fig. 4.1.6. The voltage across the UC stack and the current through the inductor are shown in Fig.16 and Fig. 17 respectively. At the beginning of the discharge period, the voltage across the UC stack is at its rated value of 700 V. UC stack starts discharging the voltage across the UC stack falls and as a result, the duty ratio of the converter also varies which results in an increase in inductor current (as shown in Figure)

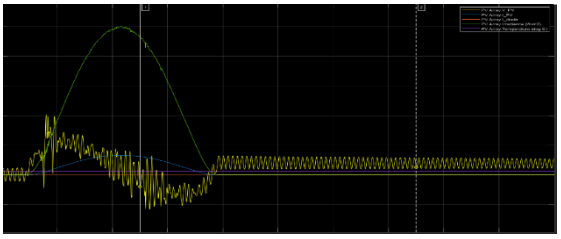


Figure 11:PV output without the proposed configuration

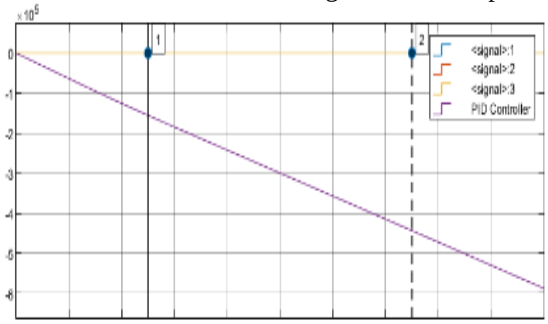


Figure 12: Harmoincs curve of LCL filters

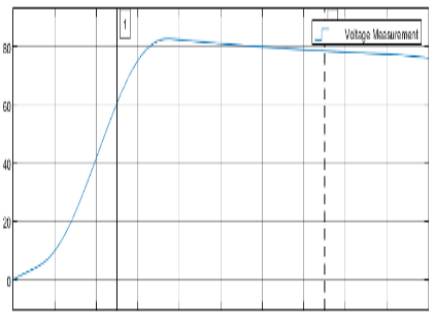


Figure 13: PV voltage curve

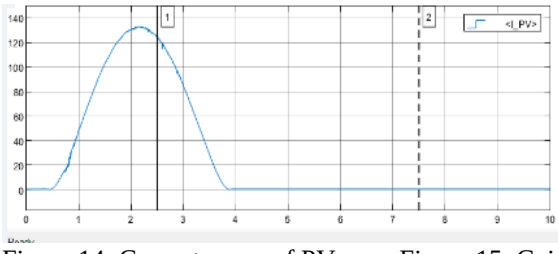


Figure 14: Current curve of PV

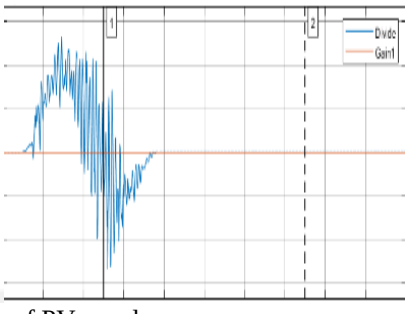


Figure 15: Gain of PV panel

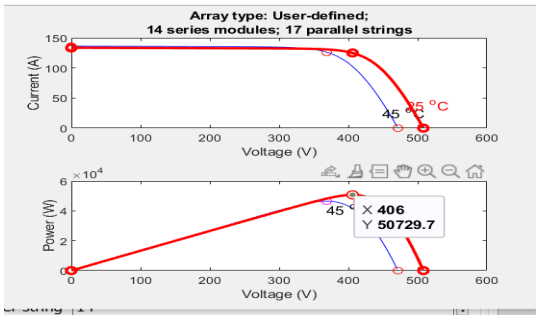


Figure 16: Power at the maximum power point

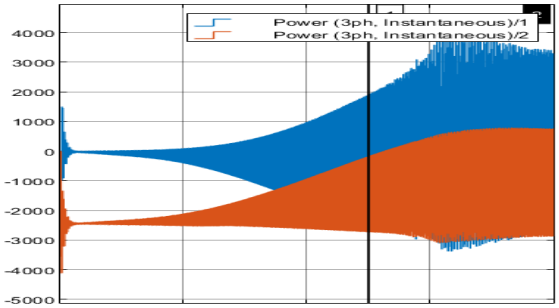


Figure 17: PV output with Ultra capacitor

The above figure 11 shows the direct output from the PV panel. Here the power the maximum power point curve is 406 W. From the below figure it is evident that the active and reactive power of the PV system is increased to a great extend with the help of the proposed system. Here we can see the active power is enhanced up to 4000 W and we can say that with the help of the proposed approach, the pv output is increased almost 10 times of the intial pv output. The MPPT algorithm used here is incremental conductance. It tracks the MPP by comparing the instantaneous and incremental conductance of the PV array. The issue of INC method is similar to P&O. The fixed step size is usually adopted, which determines the accuracy and response speed of MPPT.In the second set of simulations, the performance of the PV system 1 under shallow voltage dips is highlighted. In the case of weak grids, such dips can happen even due to a sudden increase in loads. To create a shallow voltage dip, the load (which was initially at 45 kW) is increased by 37 kW (for a small time) with the solar irradiance assumed to be 50%. In practice, where there are large sources, this increase in load will be shared in accordance with the droop settings Since the voltage dip is shallow (combined with the fact that the inverter is rated based on constant active current criterion), the inverter can process the same amount of active power (as generated by the PV panel) without violating the current limits as shown in Fig.17

VI. CONCLUSION

This work proposes a unique method to develop a PHOTOVOLTAIC- ULTRA CAPACITOR (PV-UC) configuration for the efficient working of grid connected PV systems. At the same time, there should be a good co-ordination of the photovoltaic system and ultra capacitors so as to effectively tackle the challenges arising due to sudden changes in solar irradiance and the presence of low voltages at PCC. The Test results using MATLAB SIMULATIONS indicated that in operating conditions such as sudden changes in solar irradiance, the UC stack can be effectively controlled to ensure that the net injected power into the grid is unaffected. In the presence of low voltages at the point of common coupling, the UC stack can be controlled to inject/absorb additional active power into the grid with the help of PV-UC configuration. Whenever there is a shallow voltage dip, UC injects more active power resulting in an improvement in voltage at the PCC .Since the control of UC stack ensures the power balance, the DC link voltage stays around the rated value even under low voltages.If the duration of dip is severe, the UC stack would have charged to its rated value forcing the bidirectional converter to transit from state S1 to S2. In such a scenario, the PV system must be operated in a conventional multi-mode operation. As compared to PV-battery configuration, a PV-UC configuration is a more efficient solution for handling fast moving clouds and temporary low voltages at the PCC .All the above points are tested and verified using MATLAB simulation outputs

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