International Journal of Research in Engineering and Science (IJRES)
ISSN (Online): 2320-9364, ISSN (Print): 2320-9356
www.ijres.org Volume 9 Issue 8 ǁ 2021 ǁ PP. 56-65

Design of a Read-Only Memory (ROM) creating square of an input using Threshold Logic Technology

Anup Kumar Biswas
Department of Computer Science and Engineering
Kalyani Govt. Engineering College, Kalyani,
Nadia-741235, West Bengal, India

ABSTRACT
In this paper we will concentrate our attention on creating a Read-Only Memory (ROM) on the basis of single electron tunneling junction based threshold logic gates (TLG). Some simple and complex TLG based circuits have been discussed analytically and implemented them as well. By dint of these implemented circuits, a ROM (8×4) is built up. With the help of thisROM and two other auxiliary terminals, a square generator of the 3-input binary numbers is presented. For verification purpose of square generator circuit, simulation test with the help of SIMON is done. For creating the logic circuits, we have a glance at a generic linear threshold gate by which a logic gate having many inputs and one output can be constructed. Threshold networks and truth tables are given in parallel in due places. State space diagram, linearly separable tests whether a function is linearly separable or not are discussed. At last, how many elements required for a TLG circuit,their processing delays and power consumption are listed.In addition, the curves regarding Delay vs. Error Probability and Delay vs. capacitance are provided. The comparison between the delays of MOS based circuits with other SET-based gate circuits is given in tabular form.

Keywords*: ROM, Threshold-logic, square, tunneling, Multiple-input logic gate*

Date of Submission: 18-07-2021 Date of acceptance: 04-08-2021

I. INTRODUCTION

AROMisamemorystoragedevicewhichpermanentbinaryinformationcan be stored in or retrieved from.The researcher should specify binary information which isthenfixed firmlyintheunittocreatetherequiredinterconnectionpattern.ROMsare associated withspecialinternalelectronicfuseswhich areprogrammed foran arrangement for an identifiedconfiguration.When thispatternisestablished,informationstay(s)thereineventhoughpoweristurnedoffandonagain.

Ablockdiagramofa (2^n ×m)ROMisgiveninFig. 1.Itcomprises*n*inputterminals and*m*outputterminals.Eachbitcombinationofn bits inputissaid to bean*address*andeachbitcombination thatresult fromtheoutput linesiscalled a *word.* Thenumberofbitsperwordis the same asthenumberofoutputlines*m.*Anaddressisabinarynumberthatindicatesoneofthe*minterms* or *standard products*of*n*variables.Thenumberofdifferentaddressesin the input side with*n*inputvariablesis*2^n*.We can select an output word when a particular unique address is applied,andsincethereare2^ndifferentaddresses inaROM,theremust be2^nmember of different wordsstoredintheunit.Thewordwhich isavailableattheoutputterminals/linesatanyparticulartimereliesonthe address valueappliedtotheinputterminals.AROMis individualizedbythenumberofwords(2^n)andby thenumberofbitsperword(m).

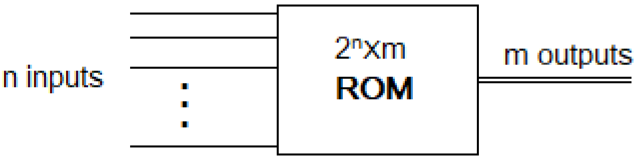


Fig.1 block diagram of a ROM

We take a 64×8 ROM. It consists of 64 words of 8 bits each. This implies that there are 8 output lines and 64 different words stored in the ROM, each of themcan be set to the output terminals. For a particular word, we want to select, will be present on the output terminals only if we determine its addressby the six input lines. There are 6input variables in a 64×8 ROM as2^6=64, we can specify 64 addresses using 6 bits. For each address input, there is a unique and fixed word. Thus, if the input address is 00100, the word number 4 is specified and it becomes visible on the output lines. If the input address is 11000, word number 24 is selected and sent to the output lines. Thereremains64-2=62 other addresses and hey can select the other 62 words.

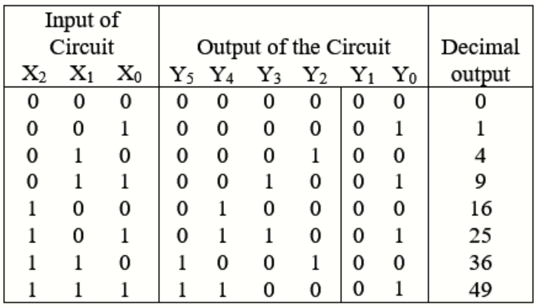
We specify aROMusingthetotalnumberofbitsitincludes,whichis$2^n \times m$.Forexample,a1024-bitROMmaybeorganizedas256wordsof4bitseach.The meaning of it is that the unitbears fouroutputterminalsand8inputterminalstospecify2^8=512words.
So,themaximumnumberofbitsstoredintheunitis512 ×4=2048.
With reference to the inner structure,theROMisacombinationalcircuitwithA NDgatesconnectedasadecoderandm-numberofORgates intheunit.
TheROMisatwo-levelimplementationinsumofstandard products (minterms)form.ItdoesnothavetobecomeanAND-ORimplementation,butitcanbeanyotherpossibletwo-levelstandard productsimplementation.ROMshavemany differentially importantapplicationsinthedesignofa digitalcomputersystem.Theuseforimplementingmorecomplexcombinationalcircuitsisoneofthe applications[14].

II. DESIGN OF A READ-ONLY MEMORY

We are interested in designingacombinationalcircuitusingaROM. This combinational circuit performs an operationthat creates a square number with respect to an input number.Thecircuitwilltakea3-bitinputvariables anddeliversa binary number to output terminalsequaltothesquareoftheinputnumber.

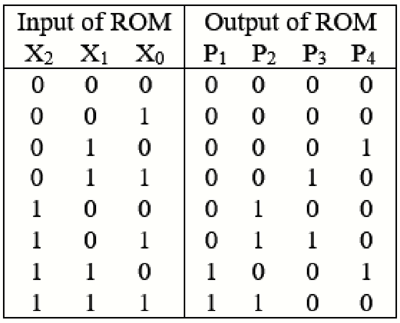
In the firststep, we aretoderivethetruthtableforthecombinationalcircuit.Wecantry to make a suitabletruthtablefortheROMbyusing particularpropertiesforthecombinationalcircuit. The truthtableforthecombinationalcircuitis depicted in Table-1.There are 3 inputsand6outputsneededto beaccommodatedallpossiblenumbers.Noted that the output Y_0 is always equal to input A_0; so it is not required to createY_0 with a ROM as it is the same as an input variable. Moreover, output $Y_1$is always 0, so this output is well-known. So, it is clear that actually our need is to generate only four outputs with the ROM; the extra two bits are easily obtained. The minimum-size of ROM we shall select must have 3 inputs and 4 outputs. 3 inputs signify eight words, therefore the ROM size must be $2^3 \times 4 = 8 \times 4$. The ROM implementation is shown in Fig. 2. The three inputs indicates that there beingeight words and every word is having 4 bits. The other two outputs for the combinational circuit are equal to 0 and Y_0. The truth table in this regard shown in Table-2. The table specifies all the information needed for programming the ROM, and the block diagram in Fig.2 shows therequiredconnections[14].

Table-1



Input of Circuit			Output of the Circuit						Decimal output
X_2	X_1	X_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

Table-2



Input of ROM			Output of ROM			
X_2	X_1	X_0	P_1	P_2	P_3	P_4
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

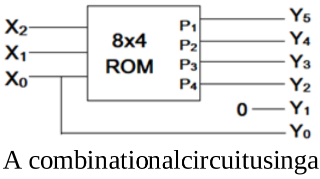


Fig. 2 A combinationalcircuitusingaROM.

Now with the help of Table-1 we can write the input-output relationships by means of the input variables X_2, X_1, X_0 and output variables Y_5, Y_4, Y_3, Y_2, Y_1, and Y_0. Six logical expressions are written as below.

$Y_5 = X_2X_1\bar{X}_0 + X_2X_1X_0 = X_2X_1$………………….. (1)

$Y_4 = X_2\bar{X}_1\bar{X}_0 + X_2\bar{X}_1X_0 + X_2X_1X_0$

$= X_2\bar{X}_1\bar{X}_0 + X_2\bar{X}_1X_0 + X_2\bar{X}_1X_0 + X_2X_1X_0$

$= X_2\bar{X}_1(\bar{X}_0 + X_0) + X_2X_0(\bar{X}_1 + X_1)$

$= X_2\bar{X}_1 + X_2X_0$ ……………………………. … (2)

$= X_2(\bar{X}_1 + X_0)$

$$
\begin{aligned}
Y_3 &= \bar{X}_2X_1X_0 + X_2\bar{X}_1X_0\\
&= (\bar{X}_2X_1 + X_2\bar{X}_1)X_0\\
&=(X_1\oplus X_2)X_0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)
\end{aligned}
$$

$$
\begin{aligned}
Y_2 &= \bar{X}_2X_1\bar{X}_0 + X_2X_1\bar{X}_0\\
&= (\bar{X}_2 + X_2)\, X_1\bar{X}_0\\
&= X_1\bar{X}_0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)\\
Y_1 &= 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)\\
Y_0 &= X_0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)
\end{aligned}
$$

Equation (1) is an expression of an AND gate, and it is anunate function. The function is linearly separable so it can be traced as a single LTG with two inputs and one output. The threshold logic expression of equation (1) is given in equation (7) [1, 2, 3, 8, 9].

$Y_5 = sgn(X_1 + X_2 - (2))$ ……………………….. (7)

2.1 2-input AND gate

For making the threshold logic gate of an AND gate, we first draw the truth table Table-3 of AND gate and compare the weighted sum of weights w_1 and w_2 of two variables X_1 and X_2respectively with the threshold value θ [1,2,3, 7, 9].

Table-3

X_1	X_2	$F(X_1X_2)$	θ	Eqn. No.
0	0	0	$0<\theta$	(1)
0	1	0	$w_2 < \theta$	(2)
1	0	0	$w_1 < \theta$	(3)
1	1	1	$w_1 + w_2 \geq \theta$	(4)

For positive logic, we assume weights of X_1 and X_2 are positive 1 each. Then from the above four inequalities in Table-3, if we assume w_1=1, w_2=1 and θ=2, then the four inequalities or equations in 5th column in this Table-3 are satisfied. Hence the Threshold logic equation for 2-input AND gate is given in equation (8) and its corresponding threshold logic gate is drawn in Fig. 3(a)

$Y_5 = sgn\{X_1 + X_2 - 2\}$……………………… (8)

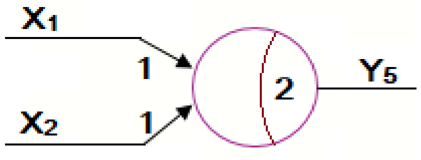


Fig. 3(a) TLG of$Y_5 = X_2X_1$

2.2 For the equation (2)

$Y_4 = X_2\bar{X}_1 + X_2X_0$ is aunate function. Now the equation will be checked whether it is linearly separable or not. From the space plot solution point in Fig.4, the black bubbles can be separated from the colorless bubbles by a plane. The black bubbles indicate that the value of $Y_4$are all 1 and colorless bubbles show the value of Y_4 equal to 0. As a plane can separate the black and colorless bubbles into two regions for the figure in Fig.4 so the function (2) is linearly separable and owing to this, the equation is suitable for drawing a single LTG to represent Y_4.

Definition: Unatefunction

AnunatefunctionisaBooleanfunctionrepresentedbyaformulasuchthateachvariableappearseitherinthepositiveorinthenegativeformthroughouttheformula.The functions$f=x_1x_2+x_1x_3+x_2x_3$isanexampleofaunatefunction.

Now. Our intention is to obtain the threshold logic function for the expression $Y_4 = X_2\bar{X}_1 + X_2X_0$. We assume that

$Y_4(X_0,\bar{X}_1,X_2) = sgn(w_0 \cdot X_0 + w_1\cdot\bar{X}_1 + w_2 \cdot X_2 - \theta)$ …………………(8)

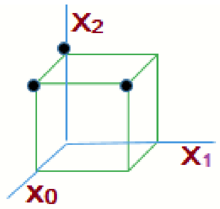


Fig. 4 Space plot of Y_4

A truth Table in support of the equations (2) and (8) is given in Table-3.

Table-3

Inputs of Y_4			$Y_4(X_0, \bar{X}_1, X_2)$	Relation of weighted sum with θ	Eqn. No.
X_2	$\bar{X}_1$	X_0			
0	0	0	0	0<θ	(i)
0	0	1	0	$w_0 < \theta$	(ii)
0	1	0	0	$w_1 < \theta$	(iii)
0	1	1	0	$w_1 + w_0 < \theta$	(iv)
1	0	0	1	$w_2 \geq \theta$	(v)
1	0	1	1	$w_2 + w_0 \geq \theta$	(vi)
1	1	0	0	$w_2 + w_1 < \theta$	(vii)
1	1	1	1	$w_2 + w_1 + w_0 \geq \theta$	(viii)

From equation (i) in Table-3, we can say that θ is a positive number, assumeθ = 2. If we put the w_0=1, w_1=−2 and w_2= 3 then all the inequalities from (i) to (viii) in Table-3 are satisfied. Hence, one solution set we have is $\{w_0, w_1, w_2 : \theta\}$ = {1, -2, 3: 2}. In equation (8), for the case $\bar{X}_1$, we are to apply the relation $\bar{X}_1$+ X_1 = 1, So $\bar{X}_1$ = −X_1 +1.

Putting these values in equation (8), we get,

$Y_4(X_0,X_1,X_2) = \text{sgn}(w_0 \cdot X_0 + w_1 \cdot (-X_1+1) + w_2 \cdot X_2 - \theta)$ …………………(8)

$= \text{sgn}(w_0 \cdot X_0 - w_1 \cdot X_1 + w_1 + w_2 \cdot X_2 - \theta)$

Again putting the solution set $\{w_0, w_1, w_2 : \theta\}$ = {1, -2, 3: 2}, we get

$Y_4(X_0,X_1,X_2) = sgn(X_0 + 2X_1 + 3X_2 - 4)$…………………..(9)

For verification the equation (9), one can put the values of (X_0, X_1, X_2) from Table-3A to the equation (9).

Table-3A

Inputs of Y4			$Y_4(X_0X_1X_2)$
X_2	X_1	X_0	
0	1	0	0
0	1	1	0
0	0	0	0
0	0	1	0
1	1	0	1
1	1	1	1
1	0	0	0
1	0	1	1

Therefore we have obtained the threshold logic equation for equation (2) and we are able to write the Threshold Logic gate for equation (9) and the corresponding diagram is given in Fig. 5.

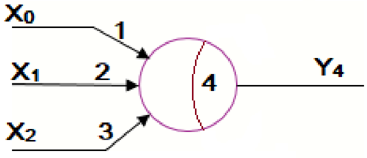


Fig. 5 TLG of $sgn(X_0 + 2X_1 + 3X_2 - 4)$

For the purpose of implementing the tunneling junction based circuit regarding the equation (9) we must find out the relevant capacitances which are essential. The values which are measured is given in Table-5.

2.3 For the Third Equation

$Y_3 = (X_1 \oplus X_2)\, X_0$ ………………………………. (3)

In this equation, there is an expression of Exclusive-OR, which is not linearly separable, as a whole the equation (3) is not linearly separable. So the Y_3 cannot be expressed with a LTG. We will not be able to construct the circuit by using two LTGs.

When we want toexpress $Y= (X_1 \oplus X_2) = (X_1 \cdot \bar{X}_2 + \bar{X}_1 \cdot X_2)$ with a threshold logic gate, first we express $P = (X_1 \cdot \bar{X}_2)$ with the help of threshold gate-based equation as given in equation (8). We can write as-

$P = sgn\,\{X_1 + \bar{X}_2 - 2\}$………………… (10)

We know $\bar{X}_2 + X_2 = 1$ or $\bar{X}_2 = -X_2 + 1$, so equation (10) will be

$P = sgn\,\{\, X_1 - X_2 - (1)\,\}$…………………… (11)

Now the Boolean expression $Y= (X_1 \oplus X_2) = (X_1 \cdot \bar{X}_2 + \bar{X}_1 \cdot X_2)$ can be written as

$Y= P + \bar{X}_1 \cdot X_2$……………………………. (12)

For finding out the threshold gate logic of equation (12), we draw the truth Table-4.There are four inequalities in 5th column in this table. Note that in equation 3 there are two variables X_1 and X_2, though it seems that P is a variable in equation (12), it would not be correct. Only two variables X_1 and X_2 are the fact and P is depending on X_1 and X_2.

Table-4

X_1	X_2	P	Y	θ
0	0	0	0	$0<\theta$
0	1	0	1	$W_2 \geq \theta$
1	0	1	1	$W_1 + W_3 \geq \theta$
1	1	0	0	$W_1 + W_2 < \theta$

After solving the inequalities in the 5th column of Table-4, we obtain a solution set $\{\, W_1, W_2, W_3; \theta\}$ = {-1, 1, 2 : 1}.Hence the Threshold equation for the Y is

$Y = sgn\{\, -X_1 + X_2 + 2P \;-\; (1)\}$……………. (13)

Last we consider the equation (3) as $Y_3 = (X_1 \oplus X_2)\, X_0 = Y\, X_0$ which is equivalent to an AND gate expression. Like a Threshold logic expression of an AND gate, we can write

$Y_3 = sgn(Y + X_0 - (2))$ ……………………. (14)

Hence combining the three equations (11), (13) and (14), we will be able to draw the threshold logic circuit of depth 3 as given in Fig.6.

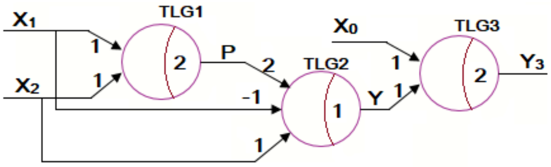


Fig.6 TLG of $Y_3 = (X_1 \oplus X_2)\, X_0$

2.4 For the equation (4)

$Y_2 = X1\bar{X}_{0},$ we observe that it is a Boolean expression of an AND gate. So according to equation (11), the threshold logic equation of $Y_2 = X_1\bar{X}_0$ will be as equation (15).

$P = sgn\,\{\, -X_0 + X_1 - (1)\,\}$…………………… (15)

And the threshold logic gate of equation (15) will be as in Fig. 7,

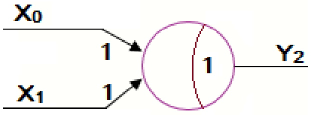


Fig.7 TLG of $Y_2 = X_1\bar{X}_0$

Based on the six equations starting from (1) to (6) we have been able to build their corresponding TLG gates for the equations from (1) to (4) and the remaining two equations (5) and (6) do not require such implementations. We have drawn the ROM based square circuit using TLGs and which is depicted in Fig.8.

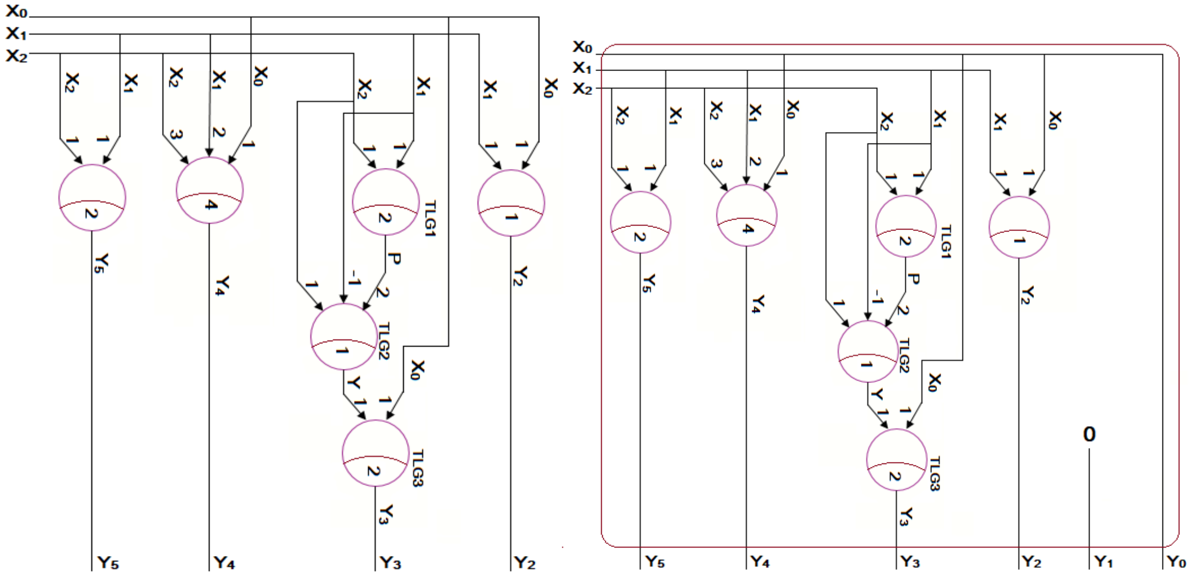


Fig. 8(a) ROM circuit of 3-inpt and 4-output ||Fig. 8(b) Square calculation circuit of 3-bit input using TLG

III. GENERAL PURPOSE MULTIPLE INPUT THRESHOLD LOGIC GATE

The figure drawn in Fig.9 is called multiple threshold logic gate [1, 2, 3, 4, 9, 10, 11] consisting of a tunnel junction having capacitance C_j and resistanceR_j, two multi-input-signals V_k^Ps and V_l^ns joined at two points ‘q’ and ‘p’ respectively. Each input voltage $V_k^P$is connected to the point “q” through their respectivecapacitances $C_k^P s$; and each other input voltageV_l^n, is joined at the point “p” through their respective capacitances C_l^ns. The supply voltage voltage V_b is connected to the point “q” through a true capacitor C_b. Junction capacitor C_j is connectedto point “p” which is connected in series withcapacitor C$_0$which isgrounded. LTGs can be constructedby means of a function presented by the signun function of h(x) expressed by equations (16a) and 16b).

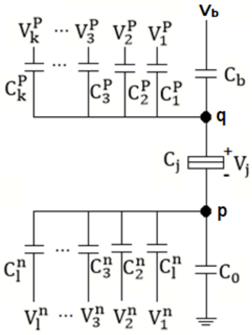


Fig.9Threshold logic gate with multi-input

$$g(x) = \text{sgn}\{h(x)\} = \begin{cases} 0, & if\ h(x) < 0 \\ 1, & if\ h(x) \geq 0 \end{cases} \cdots\cdots\cdots\cdots \text{(16a)}$$

$$h(x) = \sum_{k=1}^{n}(w_k \times x_k) - \theta \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \text{(16b)}$$

wherex_k= n-Boolean inputs and w_k being their corresponding *n* integer weights.

The LTG compares the weighted sum of the inputs $\sum_{k=1}^{n}(w_k \times x_k)$ and the threshold valueθ. When the weighted sum-value$\sum_{k=1}^{n}(w_k \times x_k)$ is greater than or equal to the threshold value θ then output of the LTG will be high (logical “1”), otherwise it will become low (logical “0”).

IV. IMPLEMENTATION OF ROM

Now we are interested in making the ROM (8×4)by using the threshold logic based on the Fig. 9. For different logic gates the values of the parameters required for them will be different. After analyzing different threshold logic expressions, the corresponding parameters are measured and found out. The list of parameters for the TLGs relevant to their threshold logic expression for the purpose of implementing the Read-only memory (ROM) are given in Table-5.

Table-5

Sl.No.	expressions	Name of Expression	Parameters
1	$Y_5 = X_2X_1$ $Y_5 = \mathit{sgn}\{X_1 + X_2 - 2\}$	2-input gate	"0"=0V, logic "1" = 16mV, $C_1^p = C_2^p = \frac{1}{2}C = 0.5aF, C_L = 9aF, C_0 = 10aF$, $C_b = 9aF, C_j = 0.25aF, R_j = 10^5\Omega$, V_b =16mV
2	$Y_4 = X_2\bar{X}_1 + X_2X_0$ $Y_4 = \mathit{sgn}(X_0 + 2X_1 + 3X_2 - 4)$	3-input gate	"0"=0V, logic "1" = 16mV, C=1aF, $C_1^p = \frac{1}{6}C C_2^p = \frac{1}{3}C$, $C_2^p = \frac{1}{2}C$=0.5aF, $C_b = 9.75aF$, $C_j = 0.25aF$, $C_L = 9aF$, $Cj = 0.25aF$, $C_0 = 10aF$, $R_j = 10^5\Omega$,. $V_b = 16.19mV$ which is close to 16mV, so $V_b = V_s$=16mV
3	$P = (X_1 \cdot \bar{X}_2)$ $P = \mathit{sgn}\{X_1 - X_2 - (1)\}$	2-input gate	"0"=0V, logic "1" = 16mV, $C_1^p = C_1^n = \frac{1}{2}C = 0.5aF$ $, C_L = 9aF, C_0 = 9.5aF$, $C_b = 9.5aF, C_j = 0.25aF$, $R_j = 10^5\Omega$, V_b =16mV
	$Y = P + \bar{X}_1 \cdot X_2$ $Y = \mathrm{sgn}\{-X_1 + X_2 + 2P - (1)\}$	3-input gate	"0"=0V, logic "1" = 16mV, $C_1^n = C_1^p = \frac{1}{2}$ $C_2^p = \frac{1}{4}C = 0.5aF, C_L = 9aF, C_0 = 9.5aF$, $C_b = 8.5aF, C_j = 0.25aF$, $R_j = 10^5\Omega$, V_b =16mV
	$Y_3 = (X_1 \oplus X_2)\, X_0 = Y\, X_0$ $Y_3 = \mathit{sgn}(Y + X_0 - (2))$	2-input gate	"0"=0V, logic "1" = 16mV, $C_1^p = C_2^p = \frac{1}{2}C = 0.5aF$ $, C_L = 9aF, C_0 = 9.5aF$, $C_b = 9.5aF$, $C_j = 0.25aF$, $R_j = 10^5\Omega$, V_b =16mV
4	$Y_2 = X_1\bar{X}_0$ $P = \mathit{sgn}\{-X_0 + X_1 - (1)\}$	2-input gate	"0"=0V, logic "1" = 16mV, $C_1^n = C_1^p = \frac{1}{2}C = 0.5aF$ $, C_L = 9aF, C_0 = 9.5aF$, $C_b = 9.5aF, C_j = 0.25aF$, $R_j = 10^5\Omega$, V_b =16mV
5	$Y_1 = 0$	--	--
5	$Y_0 = X_0$	--	--

Now we will draw and set the threshold circuit for the simulation purpose. The simulation set is given in Fig.10.

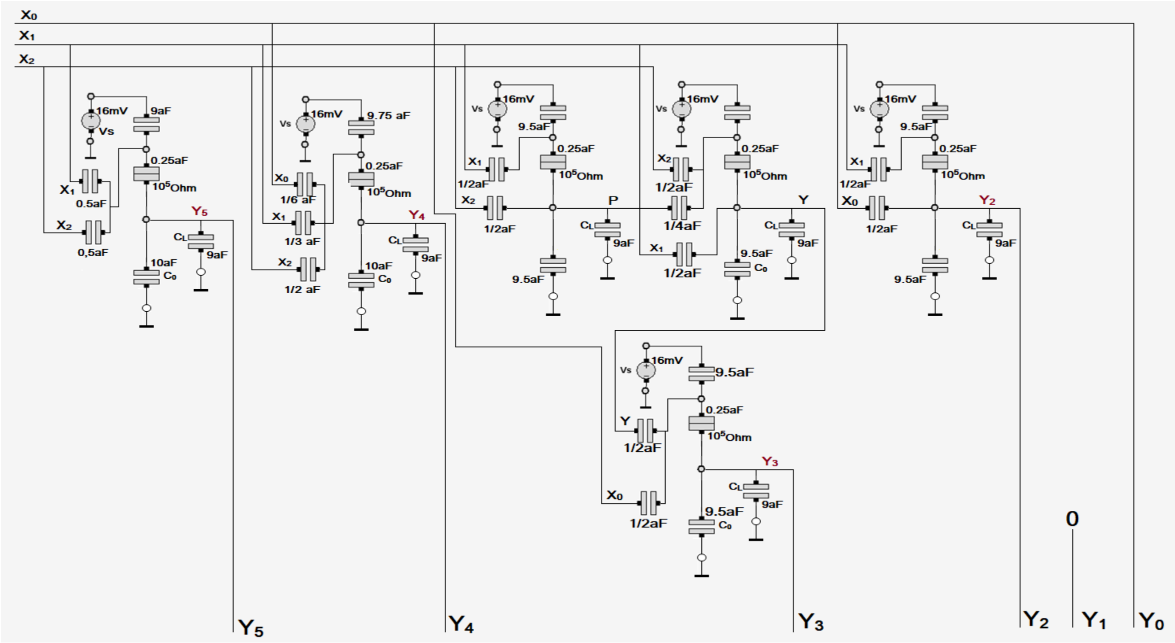
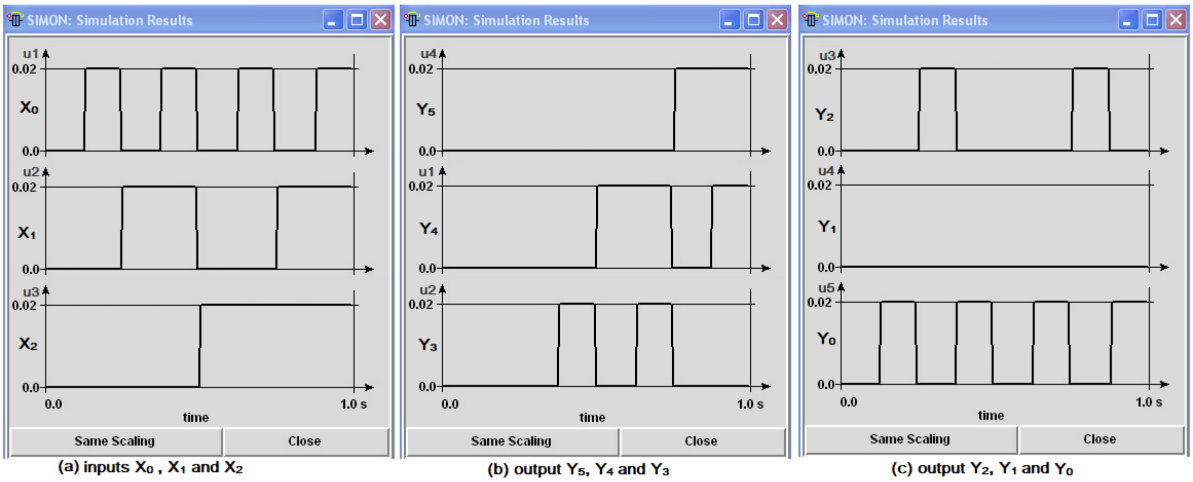


Fig. 10 Simulation set of creating square of 3-variable inputs of a ROM (8×4)

The simulation results of the Fig-10 using the simulator SIMON is provided in Fig. 10(a) below.



(a) inputs X_0, X_1 and X_2

(b) output Y_5, Y_4 and Y_3

(c) output Y_2, Y_1 and Y_0

Fig. 10(a) Simulation result of the circuit shown in Fig.10

V. Discussion

In this work we have used 2-input and 3-input threshold logic gates and we have discussed regarding AND gate, Exclusive-OR gate and more complex combinational circuits to implement (2^3× 4) ROM as well as square circuit of the three input variables. The TLG circuits are drawn after analyzing their linear separable equations. Now we must discussed about their corresponding processing delays or speed. When we are going to find out processing delays, we will involve critical voltageV_c along with the tunnel junction capacitanceC_j. The switching or processing delay in connection with a logic gate/circuit can be checked by means of the approaches [8, 9] given as follows:

Delay = $-(e|\ln\,(P_{error})|R_t)$ / ($|V_j| - V_c$) ……. (17)

Here,V_j is the junction voltage and V_c is the critical voltage and R_t is the junction resistance.

The switching/tunneling event comes to happen as soon as the tunnel junction voltage$V_j$is greater than or equal tothe critical voltageV_c, i.e., $|V_j| \geq V_c$. When this conditional equation is satisfied by a 2-input AND gate then the resulting junction voltage of the AND gate gets the value V_j =11.8mV, the internal critical voltageV_c of the tunnel junctionbecomes 11.58mV. Given that tunnel resistance $R_t = 10^5\Omega$ and the probability of error change P_{error} is equal to 10^{-12}. After measuring, the gate delay we get is 0.062|ln(P_{error}) |ns = 2.21ns. In this way we are able to find out the delays of gates and circuits listed in Table-5.

Whenever an electron passes through thetunnel junction, the total energy in the circuit gets changed. The distinct energy levels before and after the tunneling event are calculated with the equation (18).

$$\Delta E = E_{before\ tunnel} - E_{after\ tunnel}$$
$$= -e(V_c - |V_j|) \text{.........................} (18)$$

This is the switching/tunneling energy$-e(V_c - |V_j|)$being consumed whenever a tunnel event happens in the tunneling circuit. The energy consumption for different circuits is given in Table-5 as well.

Table-5

Gate/Device	elements	Delay	Switching Energy
inverter	9 elements	0.022|ln(P_{error}) | ns	10.40meV
2-input NOR	6 elements	0.060|ln(P_{error})| ns	10.70meV
2-input OR	6 elements	0.050|ln(P_{error})| ns	10.80meV
2-input NAND	6 elements	0.058|ln(P_{error}) |ns	10.70meV
2-input AND	6 elements	0.050|ln(P_{error}) |ns	10.80meV
3-input AND	7 elements	0.082|ln(P_{error}) | ns	11.58 meV
3-input NAND	7 elements	0.072|ln(P_{error}) | ns	11.58 meV
2-input XOR	13 elements	0.080|ln(P_{error})| ns	21.20 meV
3-input OR	7 elements	0.082|ln(P_{error}) | ns	11.58 meV
3-input NOR	7 elements	0.082|ln(P_{error}) | ns	11.55 meV
Y5	6 elements	0.050|ln(P_{error}) | ns	10.80meV
Y4	6 elements	0.058|ln(P_{error}) | ns	10.80meV
Y3	19 elements	0.158|ln(P_{error})| ns	32.25meV
Y2	6 elements	0.058|ln(P_{error})| ns	10.80meV
ROM (2^3× 4)	37 elements	0.158|ln(P_{error})| ns	32.25meV

We have drawn curves relating to the switching delay vs. switching error probability in Fig. 11(a) and the switching delay vs. the unit capacitance C in Fig. 11(b).

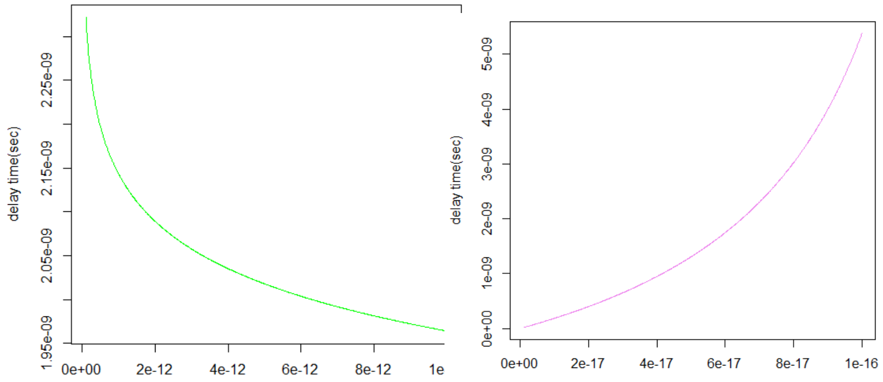
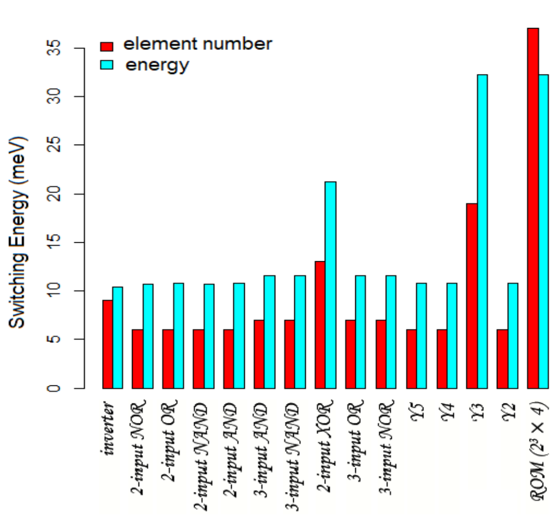


Fig. 11(a) Delay vs. Error ProbabilityFig. 11(b) Delay Vs. capacitance

We have measured / counted the total number of elements placed inany gate or circuit.We have provided the data collected from this work in connection withelement numbers, delays, and switching energy in Table-5.



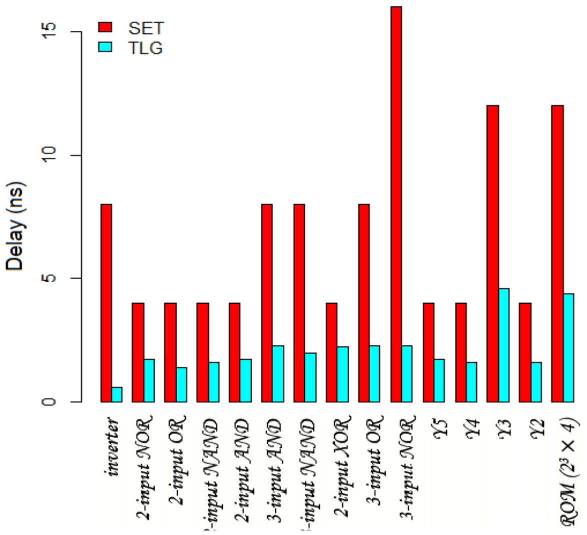


Fig. 12 comparison of Elements and switching energy Fig. 13 Bar diagram of delays of SET/TLG Vs. gates

The processing delays of distinct threshold logic circuits are different. For a 3-input OR gates, the processing delay is 0.104|ln(P_{error}) | ns, for 2-input XOR gate it becomes 0.102|ln(P_{error})| ns, and inthe (2^3× 4) ROM circuit– delay for$Y_5$is 0.062|ln(P_{error})| ns , for Y_4 =0.062|ln(P_{error})| ns, for Y_3 =0.186|ln(P_{error})| ns, and for Y_2=0.062|ln(P_{error})| ns.

Given the value of P_{error}=10^{-12}, so the time after which the first output of the $Y_3$for the ROM circuit will fan out is 0.158|ln(P_{error})| ns =4.36 ns. This is the maximum delay time for ROM (2^3× 4) also. So we are to maintain the input signal time i.e., after every 4.36 ns, we are to apply input signals. In this condition, the speed or frequency of the ROM (2^3× 4) circuit will be $1/4.36\ ns$ = 229.3MHz.

We are indeed interested in finding out the circuit delays anent CMOS, SET-based and LTG-based. The processing delay for a CMOS logic gate like AND, NAND, NOR, XOR is 12ns [15, 16], but the time required for tunneling through a single electron transistor (SET) [9, 10] is approximately 4ns [4, 5,6, 7, 12, 13].

Table-6

Gate/Device	SET-based delay ns	LTG-based delay
inverter	8	**0.60 ns**
2-input NOR	4	**1.71 ns**
2-input OR	4	**1.38 ns**
2-input NAND	4	**1.60 ns**
2-input AND	4	**1.71 ns**
3-input AND	8	**2.26 ns**

3-input NAND	8	**1.98 ns**
2-input XOR	4	**2.21 ns**
3-input OR	8	**2.26 ns**
3-input NOR	16	**2.26 ns**
Y5	4	**1.71 ns**
Y4	4	**1.60 ns**
Y3	12	**4.36 ns**
Y2	4	**1.60 ns**
ROM (2^3× 4)	12	**4.36 ns**

Switching delays of SET and LTG

Assuming the error probability is 10^{-12} , the delays for different gates/circuits we got are shown in Table-6. From the Table-6 we observe that the LTG based circuit is faster than the SET based circuit. The delays for SET and LTG gate based circuits are represented by a bar diagram in Fig13.

VI. Conclusion

ROM is an interesting device for us as the data will remain intact though power is OFF and then ON i.e. the ROM is not volatile. All the scientific data, constant numbers are stored in ROM. In the present work a square circuit for a 3 input variables, taking the help of a (2^3× 4)ROM, has been implemented. For implementing this ROM we have designed four functional units of four threshold logic expressions. After combining these four functional units and taking other two auxiliary output lines $Y_1=0$ and $Y_0=X_0$ we have drawn the full phases of the square circuit. For verification purpose, the input-output relationships are verified by using the SIMON simulator.The number of elements (single electron transistors, capacitances) used for different logic gates and other circuits, their processing delays, their power consumptions are listed in Tables. We have provided two related curves and two bar diagram for showing the relationships betweenDelay and Error Probability, Delay and capacitance, comparison of Elements and switching energy of different gates and lastly, Bar diagram of delays of SET/TLG vs. gatesIn this paper, we have visualized that the TLG based circuits are at least 2-times faster than SET based circuits. For the real operation, the temperature will be kept at 0K.

REFERENCES

[1]. Anup Kumar Biswas, "Application of single electron threshold logic gates and memory elements to an up-down Counter" International Journal of Creative Research Thoughts (IJCRT) | Volume 9, Issue 6 June 2021 | ISSN: 2320-2882

[2]. Anup Kumar Biswas, -"Implementation of A 4n-Bit Comparator based on IC Type 74L85 using Linear Threshold Gate Tunneling Technology" International Journal of Engineering Research & Technology ISSN: 2278-0181, Vol. 10 Issue 05, May-2021 pp.299-310,

[3]. Anup Kumar Biswas, "State Transition Diagram for A Pipeline Unit based on Single Electron Tunneling" International Journal of Engineering Research & Technology (IJERT) Vol. 10 Issue 04, April-2021pp.325-336, ISSN: 2278-0181

[4]. Anup Kumar Biswas, "Design of A Pipeline for A Fixed-Point Multiplication using Single Electron Tunneling Technology", International Journal of Engineering Research & Technology ISSN: 2278-0181, Vol. 10 Issue 04, April-2021 pp. 86-98,

[5]. A. K. Biswas and S. K. Sarkar: "An arithmetic logic unit of a computer based on single electron transport system" (SPQEO)Semiconductor Physics, Quantum Electronics & Opt-Electronics. 2003. Vol 6. pp 91-96 No.1,

[6]. A.K. Biswas and S. K. Sarkar: -"Error Detection and Debugging on Information in Communication System Using Single Electron Circuit Based Binary Decision Diagram." (SPQEO) Semiconductor Physics Quantum electronics and opt electronics, Vol. 6, pp.1-8, 2003

[7]. Alexander N. Korotkov, "Single-electron logic and memory devices" INT. ELECTRONICS, 1999, Vol. 86, No. 5, 511- 547

[8]. Casper Lageweg, Student Member, IEEE, SorinCot¸ofan˘a, Senior Member, IEEE, and Stamatis Vassiliadis, Fellow, IEEE "Single Electron Encoded Latches and Flip-Flops" IEEE TRANS. ON NANOTECHNOLOGY, VOL. 3, NO. 2, JUNE 2004

[9]. C. Lageweg, S. Cot¸fan˘a, and S. Vassiliadis, "A linear threshold gate implementation in single electron technology," IEEE Computer Society VLSI Workshop, Apr. 2001, pp. 93

[10]. K. Likharev, "Single-electron devices and their applications," Proc. IEEE, vol. 87, pp. 606–632, Apr. 1999.

[11]. J. R. Tucker,- "Complementary digital logic based on the Coulomb-blockade", Journal of Applied Physics., vol. 72, no. 9, pp. 4399–4413, November 1992.

[12]. Jacob. Millman and C. C. Halkias; "Integrated Electronics- Analog and Digital Circuits and Systems -second edition" McGraw Hill Education;

[13]. Millman's Electronic Devices & Circuits 4th Edition (English, Paperback, Jacob Millman)

[14]. M. Morris Mano, " Digital Logic and Computer Design" Second Edition PHI.

BIOGRAPHY

ANUP KUMAR BISWAS, born in 1971. He defended his Ph.D.[Engg.] thesis in 2005 in the stream of Electronics and Telecommunication Endineering at Jadavpur University. He was a Senior Research Fellow(SRF) in Faculty of Engineering and Technology (FET) from 2002 to 2005 at the Department of Electronics &TC. Dr. Biswas has published 26 papers in national, international journals and conferences. The area of his scientific interests are computer arithmetic, parallel architectures, nanotechnology, and computer-aided design. He is engaged in research activities and teaching last 18 years.