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A Design of Carry-Lookahead Adder with Improvised Memristor Modelling

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Abstract: *Memristor is considered widely as the fourth element which gives the relation between flux and charge, this unique property can solve the memory bottleneck problem in von Neumann Architecture. This is achieved by making storage and computation operations operate simultaneously. In this paper we are going to demonstrate basic gates using hybrid memristors. The basic gates demonstrated in this paper are "AND", "XOR" and "OR" gates. These basic gates are further used to design a 4-bit ripple carry adder and a 4 bit carry look ahead adder (CLA). All the simulations are performed in cadence virtuoso tool with 90nm technology and 1v as supply voltage.*

Keywords *– Memristor, Logic Gates, Von-Neumann Architecture, Full Adder, CLA: Carry-Lookahead Adder.*

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I. INTRODUCTION

The Moore's Law state's that number of transistors doubles every eighteen months. As this law is in the verge of meeting the physical limits of the elements, in this paper we try to explore other technology i.e., memristor based circuits.Unlike the existing basic elements, memristors functionality can be achieved by variety of time-varying functions. A new element has been theoretically introduced in 1971 by Dr. L. O. Chua. H.P labs for the first time fabricated it using titanium dioxide and platinum diode in 2008. Any device that gives relation between charge and flux is called memristor.

Memristor is a named from the conception of "memory resistor". Since memristor is not an active element, it cannot store or generate any power. The symbol of a memristor is shown in Figure below.A Memristor is two terminal passive element whichgives a relationship between charge and magnetic flux.

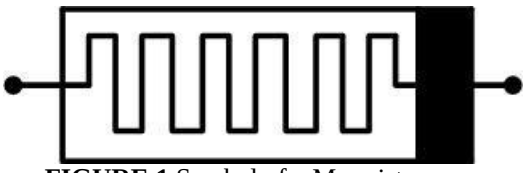

FIGURE 1. Symbol of a Memristor

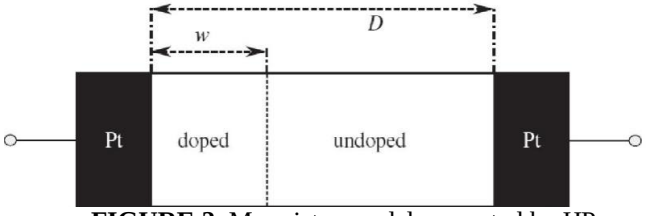

FIGURE 2. Memristor model presented by HP

In this paper we have built basic logic gates using hybrid memristor technique.The gates demonstrated are"AND" gate,"OR" gate and "XOR" gate using certain hybrid techniques.AND gate output actually depends on a single state, if any input is state 0, then the output becomes logic 0. In general, while we are designing an AND gate, we use Vdd i.e., supply voltage but through the proposed design we can achieve AND logic function without supply voltage, this in turn has few advantages like reducing complexity and lower power drain when the circuit is in a standby mode. The OR gate is designed by using a novel hybrid memristor technique, the design is made such that the inputs are given to gate terminals of the nmos and depending on these signals the nmos is either short or open in a configuration and producing the desired outputs. Here the supply voltage is taken as 1v.The XOR gate is also built by using the memristor hybrid model with the combination of nmos transistor with memristor with various stages of intermediary outputs. By using these basic gates, we have built a three input Full Adder circuit. Two kinds of full adder circuits were built both for different purposes. One for the 4-bit ripple carry adder and the other for carry look ahead adder. Two inputs are direct inputs and the third one being a carry pin. We know that the Boolean expression of full adder has two output's i.e., sum and carry. Sum expression being A⊕ B⊕ carry (Cin).In carry look ahead adder we generate carry using an external circuitry hence we do not require an inbuilt carry path while designing a full adder block. This exclusion of

carry path inbuilt helps in reducing the power whereas the carry path is included in ripple carry adder. Both will have a good impact on the overall circuitry as it is one of the most necessary digital components which is used in every addition and subtraction. Full adder is an important in both memory and computational perspective. Further, this full adder is used to build a block which does the sum and product operation of two inputs given, the sum and product operations are achieved by the gates designed using memristors, and also the full adder function, this is basically designed for convenience in design of the complex carry look ahead adder (CLA) circuit. The CLA circuit simply reduces the propagation time of the signal and maintaining consistency but the cons of this method is we get a very complicated circuit which is hard to be traced. Carry look ahead adder is designed using all these blocks and the complex carry paths are made as a symbol for convenience and to improve traceability.

II. LITERATURE SURVEY

In [1] the cell is configured using a control input signal, here the input signal is a parameter of the cell resistance, depending on this principle a common circuit is made behave as nand, nor and xor gates depending on the current it is supplied at an instance. Taking these gates further 4-bit CLA has been implemented and the improvements in area and power are observed. [2] explores the scope of hybrid memristors i.e., integration of cmos and memristor. A NOT gate has been designed using hybrid logic and DC analysis is performed to the circuit and comes to a conclusion that they are sensitive in low threshold situation. In [3] a new xor gate is proposed with 5 memristors that computes in only single step. This is further used to implement full adder. The demonstrated full adder has better speed, power and simpler architecture. In [4] a new design of xor and xnor gates is demonstrated. Only memristors are used thus enabling it to be integrable to crossbar array. In [5] a new design of binary multiplier using memristors and crossbar arrays is demonstrated. In this advantage of IMP logic is used to design a multiplier with 20 memristors and 8 computational steps. In [6] a new design of carry look ahead adder is demonstratedusing a carry chain structure method. In [7] nano device nature of memristor is used to design a better full adder. Improved parameters are speed, delay and area. 15 nmos and 15 memristors are used to build this simplified architecture. In [3] the author argues about imminent barriers of Moore's law and introduces memristor as potential solution. The relation for overall resistance w.r.to Roff and Ron is presented in [3], further explains the variable resistance property of memristor an applies this to circuits to implement AND gate, OR gate and XOR gate. All the simulations are done in PSSPICE. The proposed work is the hypothesis of what can be done using variable resistance using current flow property, but when implemented in real world it does not deliver desired results the midlevel due current division is visible while implementing. The concept of complete current diversion due to resistance becoming high or low has disadvantages of current leakage or current division. Here the optimum properties for which this theory is possible is also not mentioned. The power and delay improvements compared to traditional circuits are not claimed by the author. In [3] the single step XOR logic execution is shown as an advantage to build faster full adder but again these full adders thus designed have don't cares i.e., for some configuration the output is not what is expected. We aim to design a novel hybrid logic design that do not have any don't care scenarios, evaluate all inputs and delivers consistent output w.r.to expected output. Here we proposed design of circuits based on hybrid logic which are more efficient than traditional CMOS gates in terms of power, delay and power delay product. In this paper more reliable circuit has been proposed than the circuits in [3]. The important parameters are also compared with the traditional circuit designs.

III. PROPOSED WORK

AND gate:

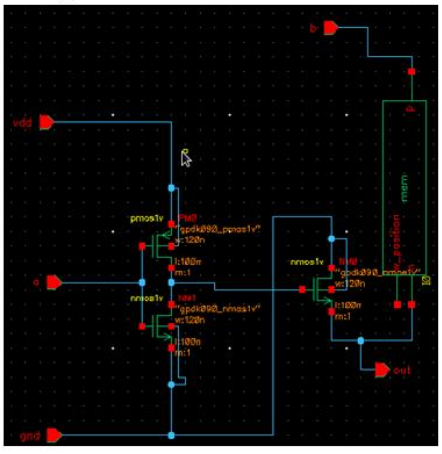

FIGURE 3. AND gate using hybrid memristor logic

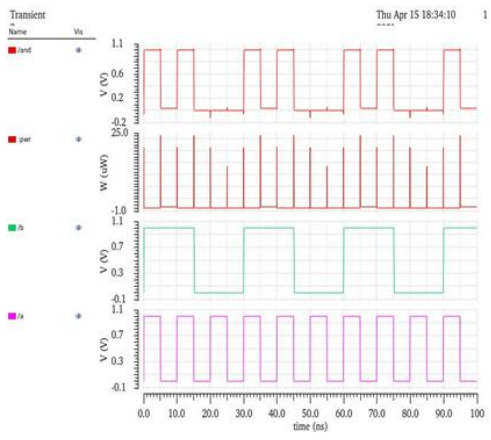

FIGURE 4. AND gate simulation graph

The "AND" gate is designed as shown in Fig 3, for 0 input at port "a" will turn on the nmos 2 thus short circuiting the output pin and the ground. This is desired output as in "AND" gate if any input is 0 the output has to be 0. If the input at port "a" is 1 the nmos is open circuited thus enabling the output to be completely dependent on signal "b", when a is 1 then output is same as "b". The output shows 1 only if both "a" and "b" are 1, this is the necessary condition of "AND" logic gate. The recent output value is always stored in the memristor.

XOR gate:

The below shown schematic is the design of the "XOR" logic gates using memristor logic. The output equation say "C" is as follows for inputs "A" and "B".

$$C = A^{1}B + B^{1}A$$

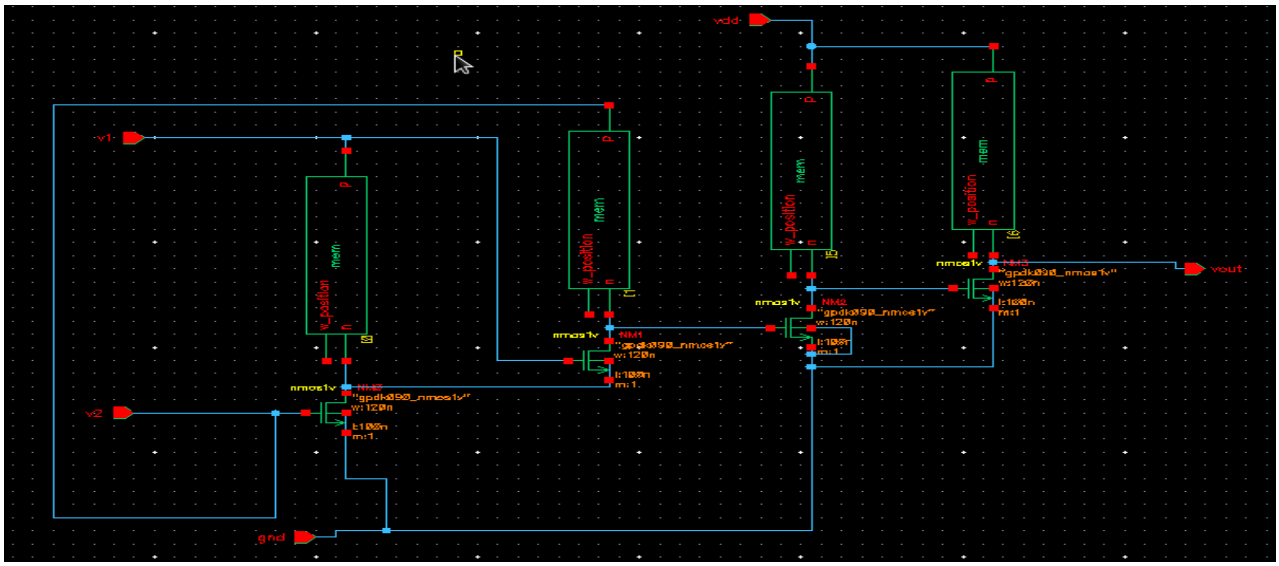

FIGURE 7. XOR gate using hybrid memristor logic

OR gate:

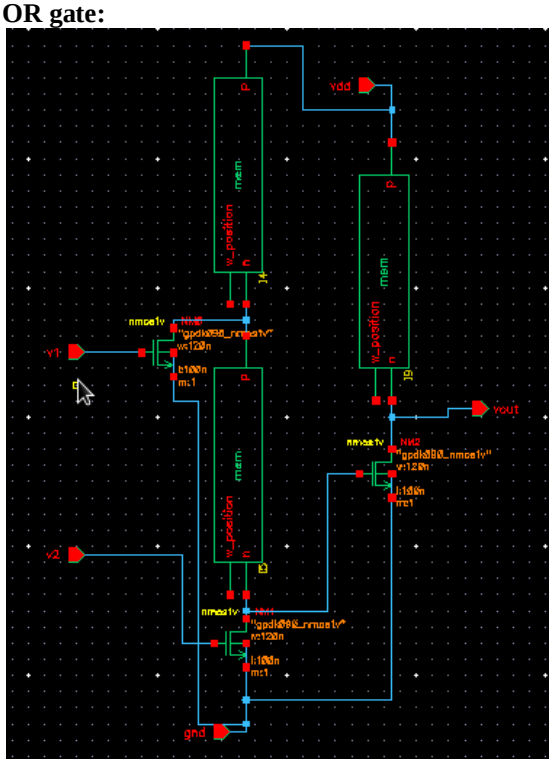

FIGURE 4. OR gate using hybrid memristor logic

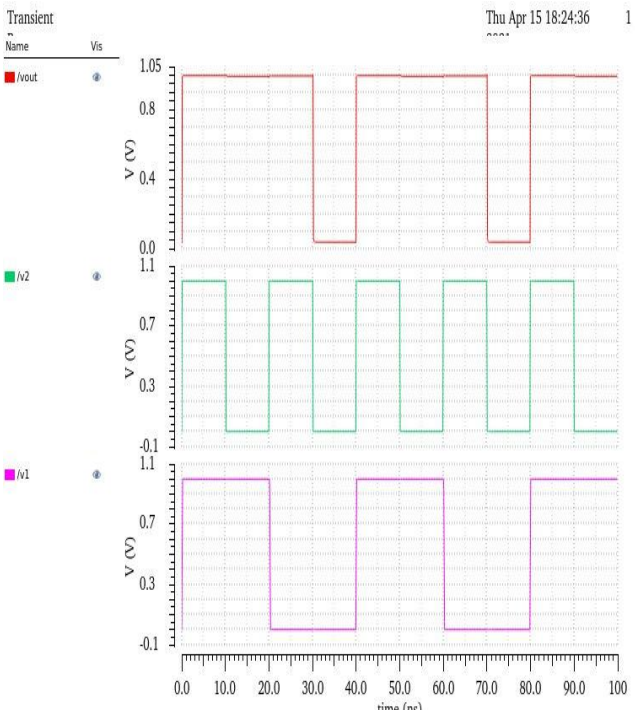

FIGURE 5. OR gate simulation graph

The "OR" gate is designed using combination of three memristors and three nmos. Whenever v1 is 1 first memristor output is grounded then input to second memristor becomes 0, This 0 in turn goes to gate of nmos 3 thus making the output as 1. Whenever v2 is 1 again the gate of nmos 3 is grounded and the output is Vdd. If any of the either inputs when made 1 the output becomes 1 thus achieving necessary condition for "OR" logic.

Full Adder for 4-bit Ripple carry adder:

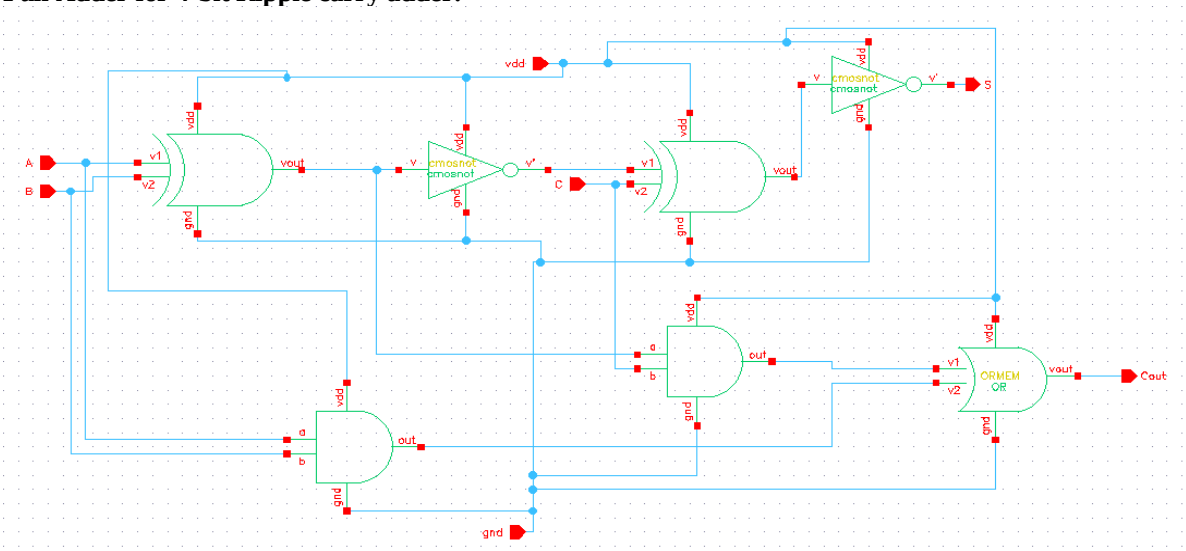

FIGURE 8. Full Adder for 4-bit ripple carry adder

This full adder is designed with the memristor based logic gates that have been explained above. The sum expression of general full adder is S = A⊕ B⊕ carry (Cin). In the above design to achieve this logic, extra two "NOT" gates have been introduced in the sum path because of signal distortion. These NOT gates amplify the signal in between but the overall desired functionality of the sum path remains the same. Carry equation above is Cout = (Cin (A⊕ B) + (A.B)).

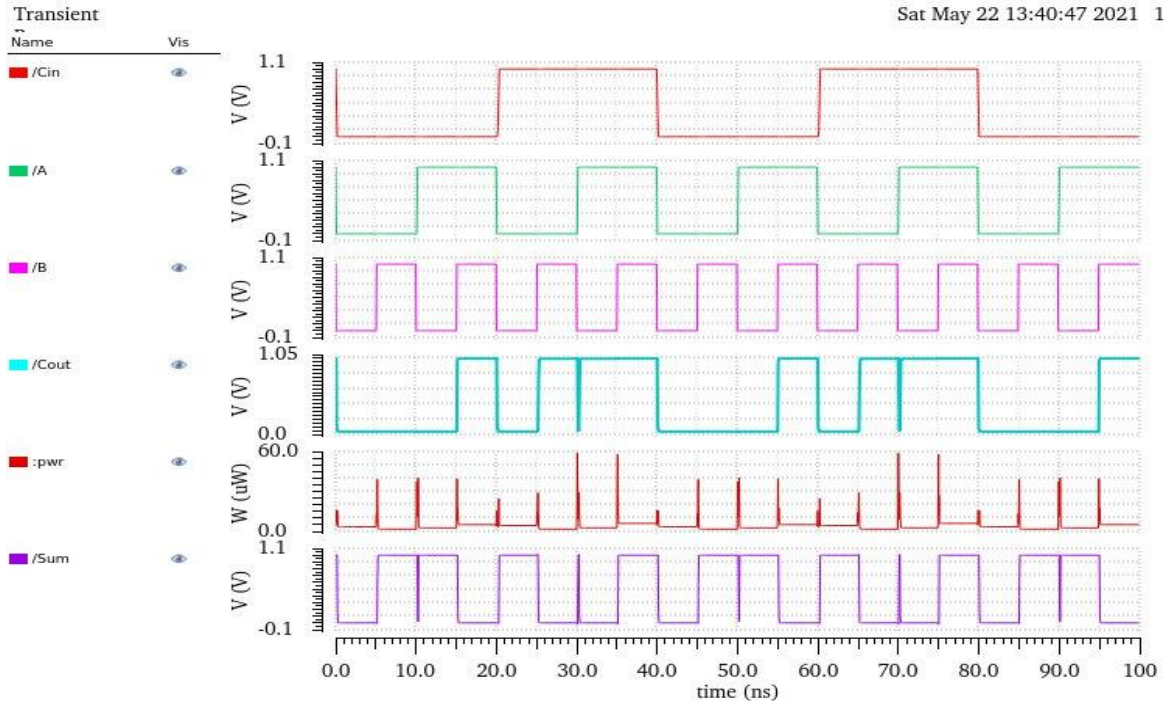

FIGURE 9. Full Adder using memristor gates graph

4-bit Ripple Carry Adder:

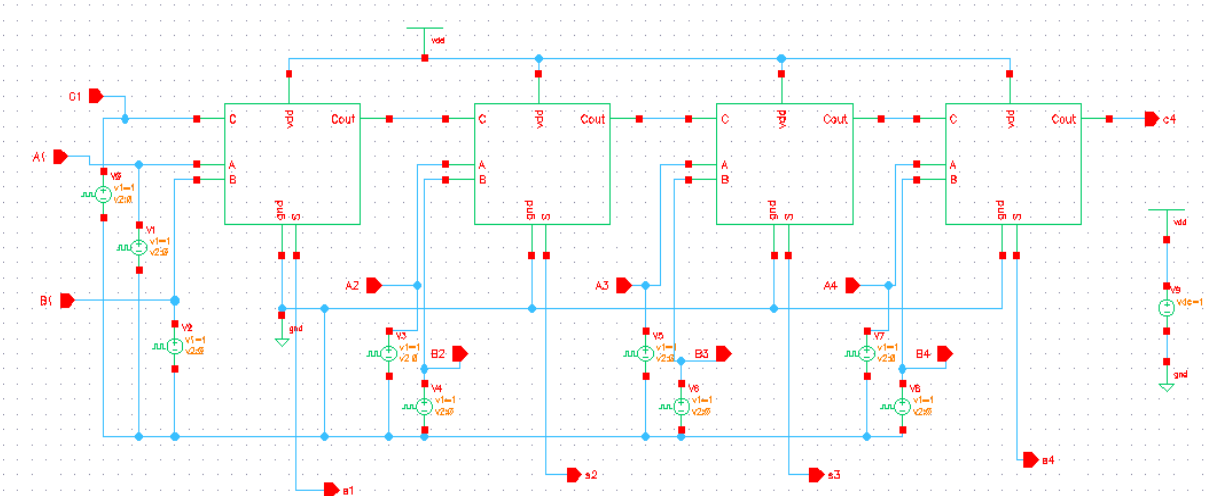

FIGURE 10. 4-bit ripple carry adder

The above schematic performs addition of two binary 4-bit inputs and thus giving the resultant output in terms of sum bits and "c4" bit. Each full adder blocks gives a sum bit and carry bit as their output. The carry bit output is given to next stage input as Cin, onlythe last state carry is considered as the output.

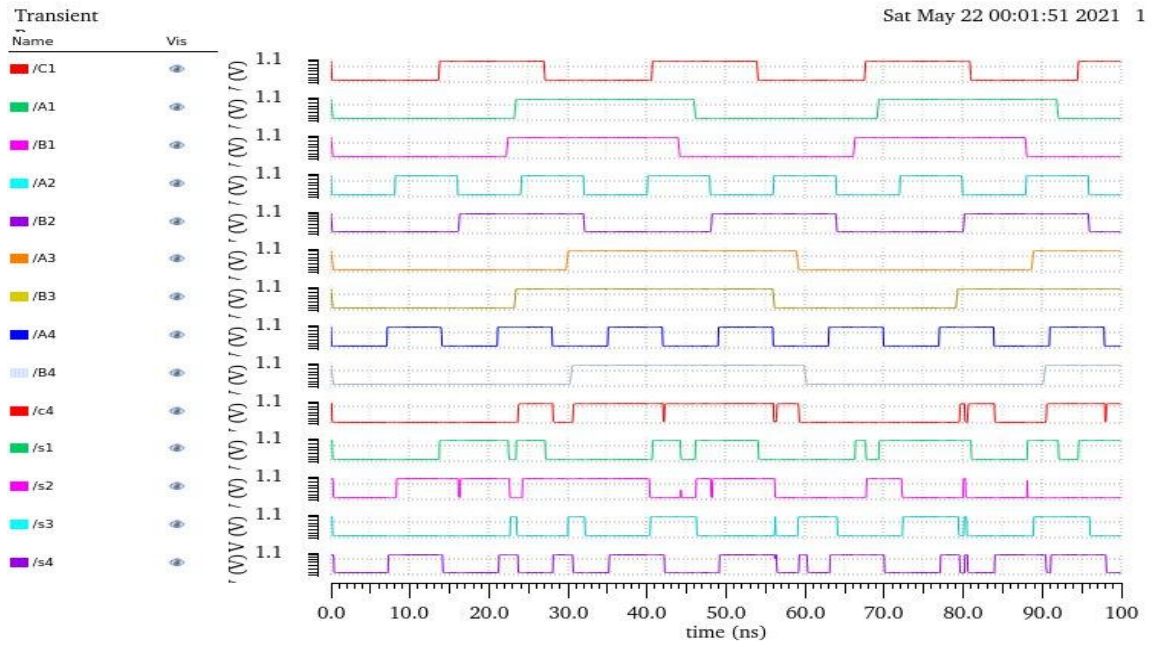

FIGURE 11. 4-bit ripple carry adder graph

Full Adder for carry look ahead adder:

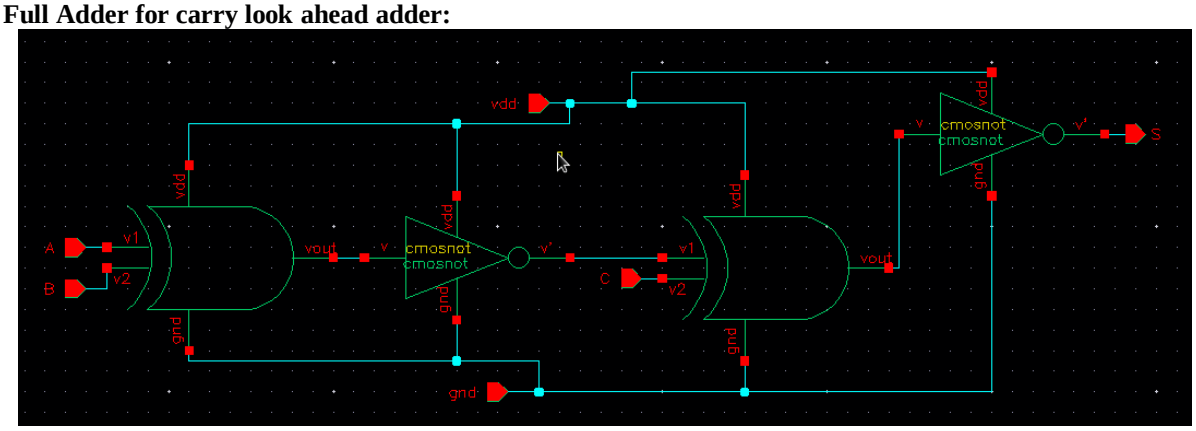

Figure 12. Full adder for CLA

In the case of CLA we don't need an inbuilt carry path inside full adder block as we generate carry independent of the full adder block. Hence this removal of carry path results in relatively low power consumption.

Carry look ahead adder (CLA):

The motivation behind the Carry Look-Ahead Adder is that in ripple carry adders, the two bits to be added are immediately available for each adder block. Each adder block, on the other hand, waits for the carry from the previous block. As a result, once the input carry is determined, it is impossible to generate the sum and carry of any block. The (n-1) th block produces the carry while the n th block waits. As a result, there will be a significant time delay due to carry propagation delay.

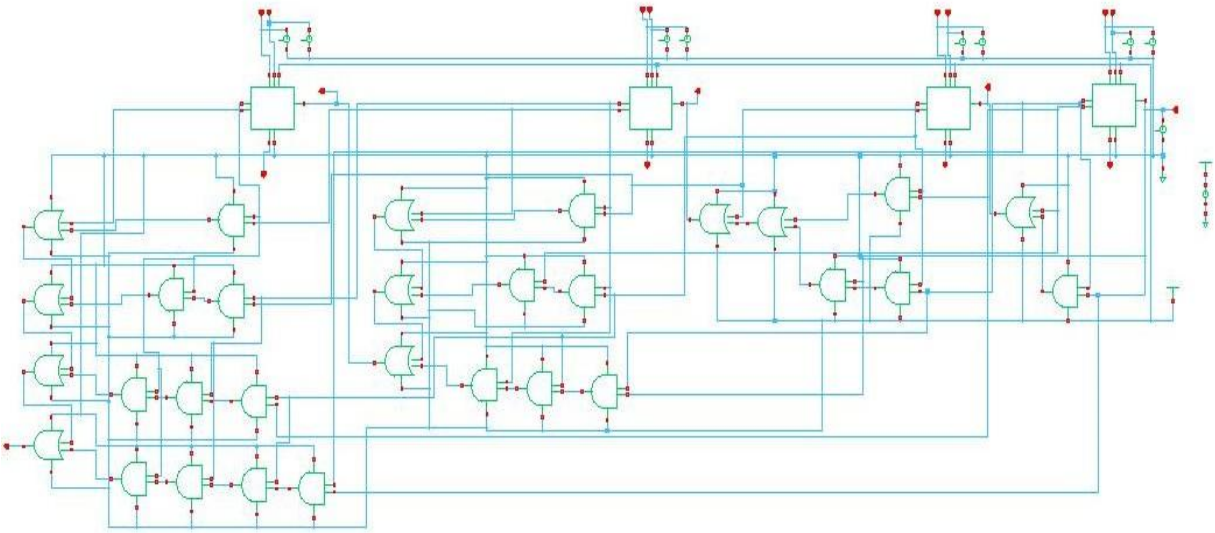

Figure 12. Carry look ahead adder using memristor schematic

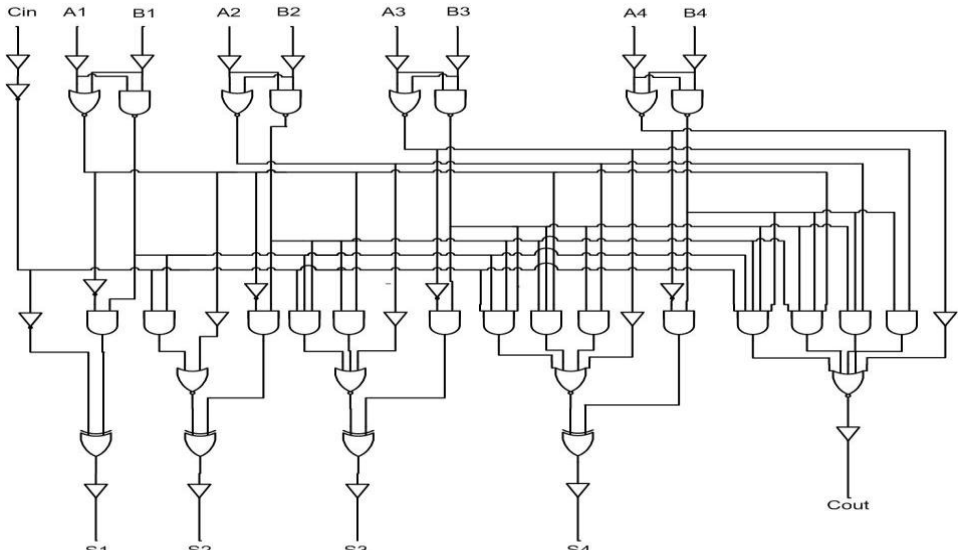

Figure 13: Gate level circuit of CLA

By implementing this design of carry look ahead adder using memristor gates we have achieved a significant improvement of 56% reduction in delay. This improved parameter comes with a cost of power and area. Power compensation is around 2.6 times the ripple carry adder using memristor circuit. This circuit could be preferred for applications where speed is at most priority.

IV. SIMULATIONRESULTS

The results obtained clearly shows that memristor based design have better power efficiency than traditional cmos designs consistently. Delay is better for memristor based circuits in most of the cases. We are able to provide convincingly better PDP values for memristor based circuit designs. All the power and delay calculations are done using cadence virtuoso calculator. PDP is obtained by multiplication of these two readings.

CIRCUIT	MEMRISTOR			CMOS		
	Delay(sec)	Power(watts)	PDP (joules)	Delay (sec)	Power(watts)	PDP (joules)
AND	10n	176n	1.76×10^{-15}	2n	45n	9×10^{-17}
OR	0.2n	3.5n	7.10×10^{-17}	6.4n	184µ	1.2×10^{-12}
XOR	11.9n	1.4µ	1.7×10^{-14}	29n	210µ	6.1×10^{-12}
Full adder without carry	0.29n	3.22µ	9.32×10^{-16}	0.1n	1.3m	1.3×10^{-13}
Full adder with carry	6.4n	3.86µ	2.47×10^{-16}	0.1n	1.3m	1.3×10^{-13}
RPA	44.5n	18.33µ	8.15×10^{-13}	92n	99µ	9.1×10^{-12}
CLA	20n	48µ	9.6×10^{-13}	47n	170µ	7.9×10^{-12}

V. CONCLUSION

In this paper we have successfully designed improvised circuits with the hybrid memristor logic. These circuits are basic elements of an ALU. It could also be used for various other general applications as well. We have achieved 71.7%, 81% improvement in power consumption of carry look ahead adder and ripple carry adder respectively. There is a significant improvement in terms of delay in most cases. The overall power delay product had significantly improved. Hence the benefits of memristor based gates can overcome the challenges of later CMOS full adder.

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