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Review of Multilevel Inverter Technologies

Abstract— *This paper provides an overview and study of multi-level topologies and various control mechanisms for modulation. Multilevel power conversion technology is an option to reach requirements with high power medium voltage. In this region, the H Bridge is analyzed for multiple inverter topologies such as diode clamped, flying condensers, as well as their advantages and disadvantages.*
Keywords— *Multilevel inverter, topology, DCMI,PWM.*

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I. Introduction

Inverter is an electronic control unit that converts the DC voltage into AC voltage. Because of expense and device sophistication, inverter technology was not commonly utilized in industrial applications until the 1960s. Later on, the inverter concept was greatly developed and implemented in the new industrial revolution. Nabae first suggested multi-level inverters in 1980 and introduced them at the IEEE International Conference[1]. The source of DC used in the inverter usually is the battery or operated output of the rectifier. The inverter output tension is regulated primarily with switches that produce AC power in square wave, square wave or sine wave [2-3]. The inverters may be categorized as square wave inverters, almost square wave inverters, two-level PWM inverters and multi-level inverters, according to the design of the output wave form[4]. These can be seen in Fig.1. In high power and low voltage conditions, the Multilevel Inverter (MI) system has been implemented as an option. A MI's basic concept is to use power semiconductor switches and several lower voltage DCs to perform the power conversion by synthesis of the waveform staircase voltage. In Batteries, and capacitors multiple input DC rates may be used for clean energy sources. Power switches are regulated to combine these several input DC values to reach a high output voltage, although the measured voltage of the current semiconductor switches depends on the DC power source value. Therefore, the voltage load on a control switch is usually much smaller than the voltage.

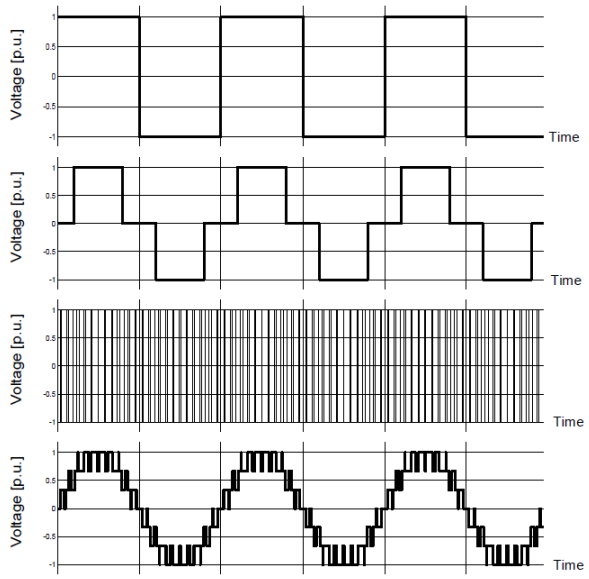

Fig. 1 Various inverter waveform (a) Square wave; (b) Quasi-square wave; (c) Two-level PWM waveform; and (d) Multilevel PWM waveform

II. REVIEW of multilevel inverter topologies

Major configurations of multilevel inverters used in industrial applications and listed in several literatures; cascaded H-bridges inverters with separate DC fuels, Diode Clamp and flying condensers used in small, medium and high power applications are discussed briefly.

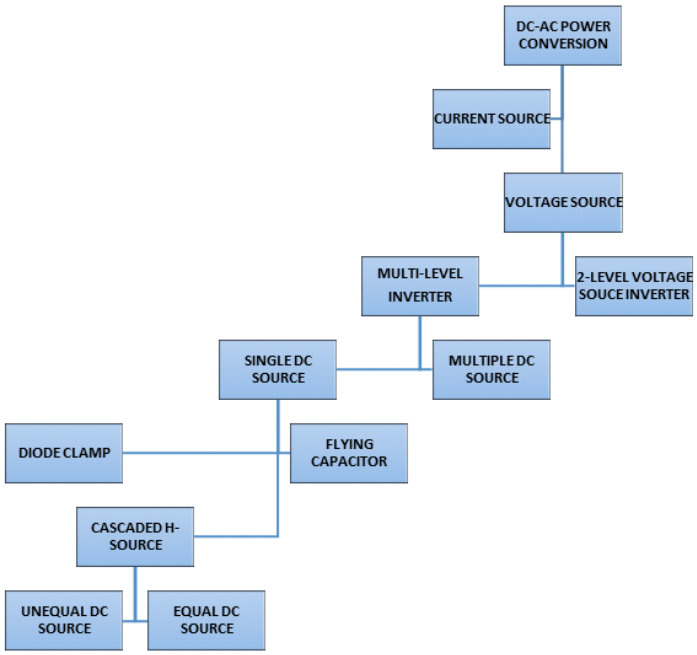

Fig 2.

A. DIODE CLAMPED MULTILEVEL INVERTER

This topology uses diodes to close the voltage that the voltage stress on power equipment is suppressed. This is the first multi-level inverter topology practically implemented. The circuit topology specification is provided below [5,6].

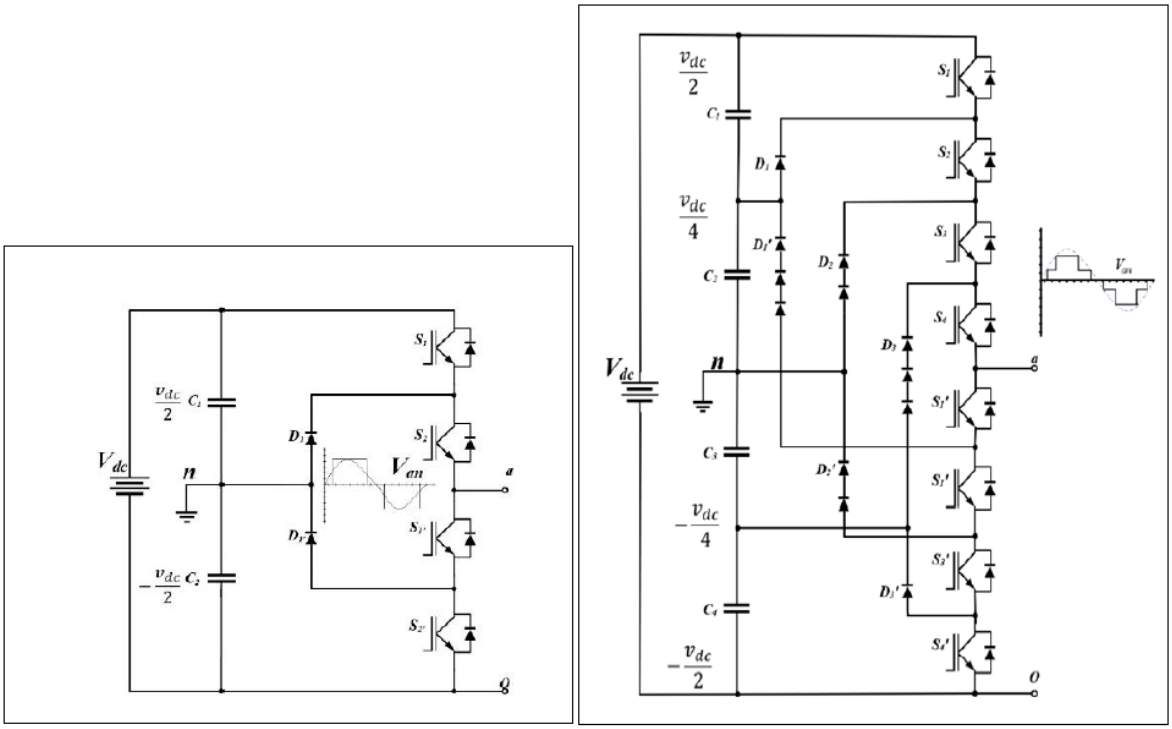

Fig 3(a) 3 Level and Fig 3(b) 5 Level Intverter

We generate more than two voltage levels on multilevel inverters, which give an almost pure waveform of the sinusoidal power . The waveform is simpler due to different voltage rates in the output, however the circuit is more complicated because of the introduction of the valves. With lower dv / dt, higher harmonic distortions[1.2]. And it also requires a complicated control system.

Number of switches for m-level= 2(m-1).

Input voltage source= (m-1).

Diodes for clamping voltage= (m-1)(m-2).

In [7] it is also addressed how FCMLI and its gate drive circuit will improve its low-cost boost pitch power supply. In [13] the soft-turn technology for the multi-stage inverter of the was introduced so that it could be expanded from three to any point. The downside of this inverter is that it has a low voltage and current value of the switching valves. Also described are architecture, function, control and switching patterns. In [7] the creation of FCMLI's low cost power supply boost trap and its gate drive circuit is addressed. Discussed In [8] the soft-turn technology for the multi-level inverter flying capacitor is suggested to expand this technology from 3 tiers to any stages. The downside of the inverter is that the shifting valves are of low voltage with a current level. The coupling inductor will achieve so. Patterns are also presented with design , operation, control, and switching.

B. Cascaded Half-Bridge based Multilevel DC Link (HBMDCL) Inverter

[50, 51] has presented a new multilevel inverter named as "Cascaded Half-Bridge based Multilevel DC Link (MLDCL) Inverter". A four input DC stage *HBMDCL* inverter can be located in Fig.7. It contains cascaded half-bridge cells, each of which has its own DC source. It has separate "level-generation" and "polarity-generation" parts. The level-generation part comprises of the sources *VDC,j* { *j* = 1,2,3,4} and the power switches *Sj* { *j* = 1 to 8}. This part synthesizes a multilevel DC voltage, *vbus(t),* fed to the "polarity-generation" part, comprising of switches *Qj*{*j* = 1 to 4},which in turn alternates the polarity to produce a multilevel AC waveform.

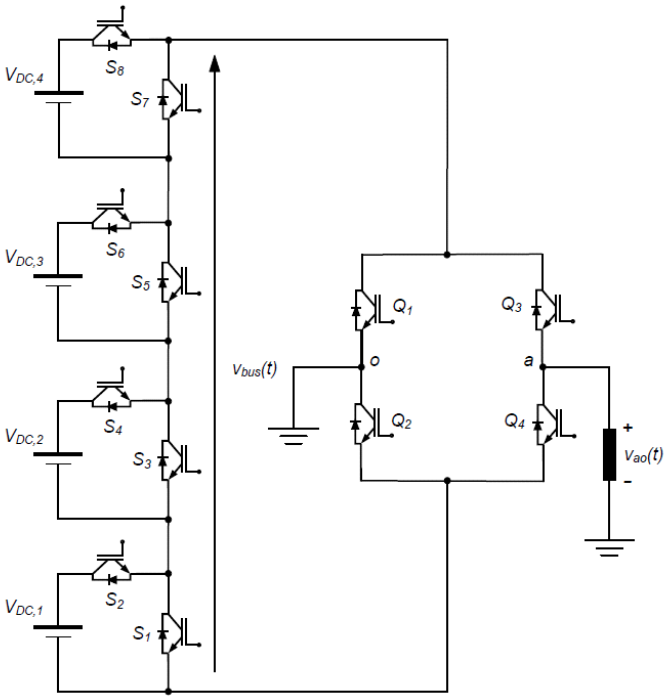

Fig 4."Cascaded Half-Bridge based Multilevel DC Link (*HBMDCL* Inverter" as proposed in [50, 51]

VALID SWITCHING STATES FOR THE "MLDCL TOPOLOGY" SHOWN IN FIG.4

State	$v_{bus}(t)$	Switches in ON state
1	$V_{DC,1}$	S_2 , S_3 , S_5 , S_7
2	$V_{DC,2}$	S_1 , S_4 , S_5 , S_7
3	$V_{DC,3}$	S_1 , S_3 , S_6 , S_7
4	$V_{DC,4}$	S_1 , S_3 , S_5 , S_8
5	$V_{DC,1} + V_{DC,2}$	S_2 , S_4 , S_5 , S_7
6	$V_{DC,1}+ V_{DC,3}$	S_2 , S_3 , S_6 , S_7
7	$V_{DC,1} + V_{DC,4}$	S_2 , S_3 , S_5 , S_8
8	$V_{DC,2} + V_{DC,3}$	S_1 , S_4 , S_6 , S_7
9	$V_{DC,2} + V_{DC,4}$	S_1 , S_4 , S_5 , S_8
10	$V_{DC,3} + V_{DC,4}$	S_1 , S_3 , S_6 , S_8
11	$V_{DC,1} + V_{DC,2}+ V_{DC,3}$	S_2 , S_4 , S_6 , S_7
12	$V_{DC,2} + V_{DC,3}+ V_{DC,4}$	S_1 , S_4 , S_6 , S_8
13	$V_{DC,1} + V_{DC,3}+ V_{DC,4}$	S_2 , S_3 , S_6 , S_8
14	$V_{DC,1} + V_{DC,2}+ V_{DC,4}$	S_2 , S_4 , S_5 , S_8
15	$V_{DC,1} + V_{DC,2}+ V_{DC,3}+ V_{DC,4}$	S_2 , S_4 , S_6 , S_8
16	0	S_1 , S_3 , S_5 , S_7

In Table I, four switches simultaneously lead for the level generation portion, and two switches for the polarity generation component, to achieve a specified amount. The topology indicates that each polarity-generation part 's power transition must have a minimum voltage. Blocking power equivalent to the cumulative voltage value of the signal. These switches are higher than the switches in the level generation portion. Because it is possible to synthesize the zero-level using polarity component switches, higher rating switches may be worked on a fundamental switching frequency.

C. Flying Capacitor Multilevel inverter

"The voltage steps defined in the flying capacitor type converter is same as that of diode clamp. The phase voltage of an m level converter has m-1 capacitors with 2m-1 steps in the line voltage." [9]

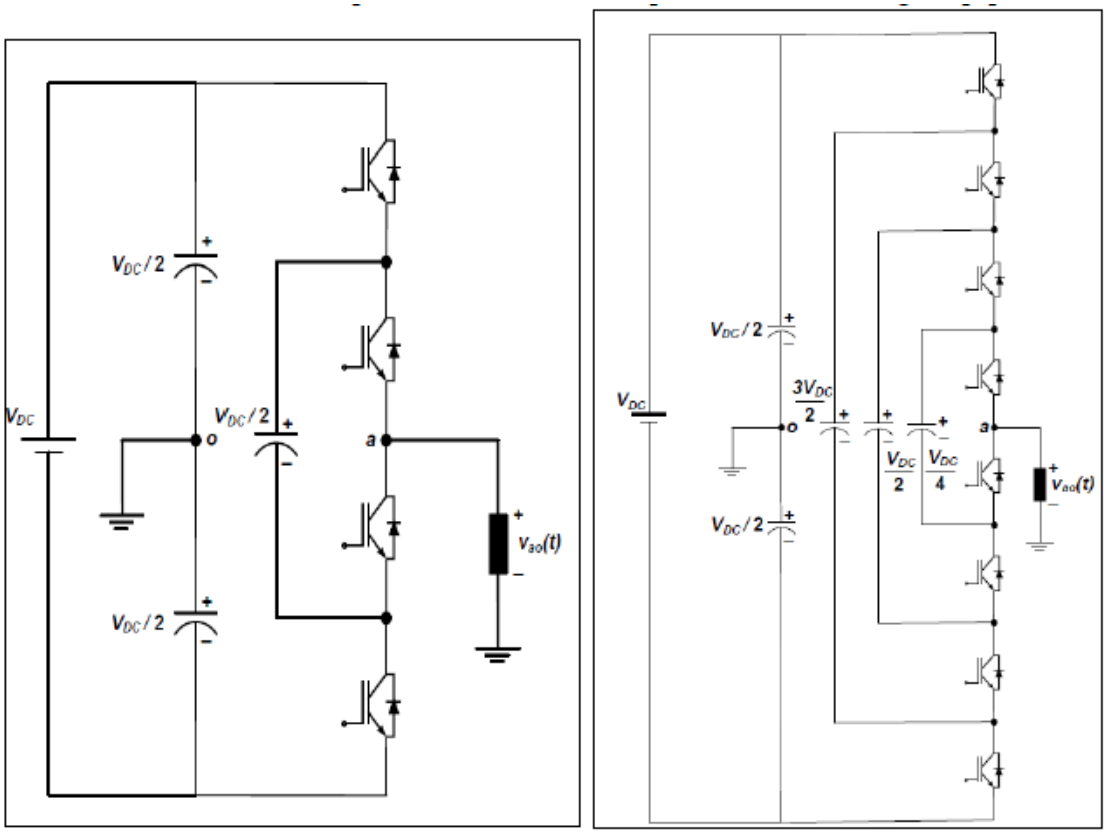

Fig 5. Three level and Five level flying capacitor.

The flying condenser may be used in the actual power conversion by careful selection of the switch combination. The underlying question is the Switch combination range and working frequency are significantly higher than the standard frequency. The following benefits and disadvantages can be summarized here[10].

Benefits

1) Big storage condenser numbers indicate extra
ride through capabilities during power outages.
2) Provides redundancy of the switch combination
Balancing different amounts of voltage.
3) Reduces the harmonic quality by rising voltage levels.
4) It is possible to control both the actual and reactive power flows.

Advantages

1) Inadequate storage condensers are available when the converter level is high, so that may be more expensive.
2) Power of the inverter is more complex.

III. CONTROL STRATEGIES

A. Pulse Width Modulation (PWM) technique

Modulated pulse width (PWM) inverters are often used in realistic applications. These inverters can produce variable magnitude and frequency ac voltages. The efficiency of the PWM inverter output voltage is higher than the square wave inverters. The PWM inverters are mostly found in ac drives at variable rpm. Through changing the frequency of the applied ac voltage, large variance in drive speed may be accomplished. A linear relationship between the applied voltage and frequency should be defined. The PWM inverters may be used in single and three phase forms. Depending on the deployment strategies, there are various forms of PWM techniques. For all these techniques, however, the output voltage produced after filtering achieves a good quality waveform for sinusoidal voltage, which is of fundamental frequency and scale. The modulation ratio [ma] is obtained from the amplitude of reference signal [Vref] with the amplitude of carrier signal [Vc](Triangular signal).

$$M_a = \frac{V_{ref}}{V_c}$$

……(1)

You may adjust the output voltage by adjusting the m_a value for different reference signal amplitudes. If m_a is less than or equal to 1, the spectrum is constant with the amplitude of the fundamental frequency and the modulation ratio. When ma is between 1 and 3.24, the range is over the region of modulation when the basic frequency amplitude does not differ linearly with the modulation ratio m_a. The harmonics in the output voltage in side bands are induced by over modulation. Other harmonic parameters used in PWM operation are Harmonic Factor (HF), Total Harmonic Distortion (THD) and Weighted THD (WTHD).

IV. Conclusion

This paper outlines the description and control methods of the inverter and multi-level inverter. Specific principles and strategies in MLI have been explored. The key emphasis is on the general overview of multi-level inverters in the current scenario and their applications. Day-to-day applications based on a multi-level inverter concept are developed. Researchers who want to work in this field need to learn the basic skills of MLI. If the researchers think about MLI, they will also try to operate as much as possible with limited switching devices and should be able to achieve strong peak voltage at a lower switching frequency. Experimental research is under way given the difficulty of systems and control circuits. It helps raising the components of power electronics and increases the overall harmonic profile and device efficiency.

References

[1]. Nabae, A., Takahashi, I., and Akagi, H. A neutral point clamped PWM inverter, Proc. IEEE APEC80 conf., 1980, pp.761-766 [20]
[2]. Agelidis VG, Balouktsis AI, Cossar C.(2008), On attaining the multiple solutions of selective harmonic elimination PWM three-level waveforms through function minimization., IEEE Trans Ind Electron ;55:9961004.
[3]. Agelidis VG, Balouktsis A, Balouktsis I. (2004), On applying a minimization technique to the harmonic elimination PWM control : the bipolar waveform. IEEE Power Electron Lett;2:414.
[4]. Chiasson JN,Tolbert LM, McKenzie KJ, Zhong D.(2004), A complete solution to the harmonic elimination problem. IEEE Trans Power Electron;19:4919.

[5]. Anjali Krishna R. and Dr L Padma suresh "A brief review on multilevel inverter topologies" Conference on Circuit,Power and Computing Technologies [ICCPCT] 2016. [1]
[6]. Nordvall "Multilevel inverter topology survey" thesis in electrical power engineering 2011.
[7]. S. A. Molepo; H. D. T. Mouton Power "A flying capacitor multilevel inverter with bootstrap- powered MOSFET gate drive circuits"Electronics Specialists Conference, 2002. pesc 02.2002 [12]
[8]. Byeong-Mun Song; Juhyung Kim; Jih-Sheng Lai; Ki-Chul Seong; Hae-Jong Kim "A multilevel soft-switching inverter with inductor coupling";Sun-Soon Park IEEE Transactions on Industry Applications Year: 2001,Volume: 37, Issue: 2 PP: 628 - 636,
[9]. IEEE 33rd Annual Year: 2002, Volume: 2 PP: 701 - 705 Gui-Jia, Su; , "Multilevel DC-link inverter," *Industry Applications, IEEE Transactions on* , vol.41, no.3, pp. 848- 854, May-June 2005. [50,51]
[10]. Gui-Jia, Su; , "Multilevel DC link inverter," *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE* , vol.2, no., pp. 806- 812 vol.2, 3-7 Oct. 2004.
[11]. José Rodríguez, Jih-Sheng Lai, Fang Zheng Peng," Multilevel Inverters: A Survey of Topologies, Controls, and Applications", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 4, AUGUST 2002
[12]. Mohd Aizuddin Yusof, Muzaidi Othman, Sze Sing Lee,M. A. Roslan and J. H. Leong, "Three-Phase Multilevel Inverter with Reduced Number of Active Power Semiconductor Switches for Solar PV Modules"IEEE.2014 2nd international conference on Electronic design (ICED),penang,Malaysia