International Journal of Research in Engineering and Science (IJRES)
ISSN (Online): 2320-9364, ISSN (Print): 2320-9356
www.ijres.org Volume 9 Issue 3 ǁ 2021 ǁ PP. 55-62

Statistical validation of a PWM algorithm based on a linear equation applied on three-phase inverter

J.C. Pérez-Merlos*[1], E. Rodríguez-Ángeles[1], A. Lambert-Lobaina[2], M. Salgado-Gallegos[1], J. Salas-García[1]

[1]*Facultad de Ingeniería, Universidad Autónoma del Estado de México, Toluca, Edo. de México, México*
[2]*Universidad Anáhuac del Norte*
*Corresponding Author:*jcjcjc63@yahoo.com*

Abstract
This work presents the statistical validation of an algorithm that generates Pulse Width Modulation (PWM) from a linear equation. It was implemented in hardware description language (VHDL) and programmed in a Field Programmable Gate Array (FPGA) of the Spartan 3E family. The algorithm allows you to vary the width of a pulse to control the trip of the transistors of a three-phase inverter. To validate the functionality of the algorithm, linear regression was used between the input analog digital converter and frequency, voltage and speed variables, taking the speed of the motor as a dependent variable and the measurement of voltage and frequency as independent variables. The results obtained were positive with an R^2 factor of .99, which allows us to conclude that the model is valid.

Keywords:*Statistical validation, Three-phase inverter, PWM, VHDL application, linear equation.*

Date of Submission: 10-03-2021 Date of acceptance: 25-03-2021

I. INTRODUCTION

A variable frequency drive is used to control the speed and torque of an induction motor. It converts a fixed line voltage and frequency to a variable voltage and frequency to power the motor input (single or three phase) [17].

The DC/AC converter, known as an inverter, is a circuit that converts a DC source to an AC sinusoidal voltage source, to power AC loads, such as induction motors[11]. In Figure 1, the electrical diagram of a three-phase inverter is shown.

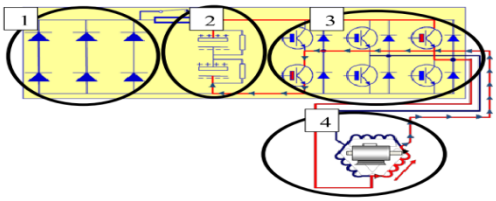

Figure 1. Electrical diagram of induction motor driver. 1) Three-phase rectifier, 2) filter, 3) three-phase inverter, 4) induction motor[8].

Patiño[14], mentions that an inverter can be classified according to its input type as: voltage source inverter (VSI), current source inverter (CSI), the latter being used only in applications with very high power AC motor drivers or in vector control drivers.

Mohammed et al. (2013), define that power electronics is the application of electronic devices for the control and conversion of electrical energy. They mention that in the future applications of the inverters, work should be done on new methods of transistor trip control algorithms, as well as new multilevel structures in converters [10].

There are a large number of works related to inverter control through digital algorithms or analog circuits that generate pulse width modulation (PWM) and that enable or disable transistors of the three-phase inverter in correct time and sequence.

Pulse Width Modulation (PWM) is used in a wide variety of applications ranging from measurements and communications to power control and conversion. In AC motor drives, the pulse width modulated inverter makes it possible to control the magnitude of voltage, current and frequency. It also supports reducing total

harmonic distortion (TDH) at the inverter output. However, the relative complexity of the control makes this modulation an onerous strategy when implemented [6].

Jimena et al. (2007), comment that since Schonung (1964) stated that the harmonic content in the operation of an inverter can be significantly improved by modulating as a function of a sinusoidal signal and proposed the algorithm of Sine Pulse Width Modulation (SPWM), with this development of modern PWM algorithms started [5].

As mentioned, Pulse Width Modulation (PWM) provides a method of decreasing the Total Harmonic Distortion (TDH) factor of the load current. An output from a PWM inverter, with some filtering, generally meets TDH specifications more easily than the square-wave switching scheme. The unfiltered PWM output will have a relatively high TDH factor, but the harmonics will have much higher frequencies than the square wave, making filtering easier [3].

Rashid (2015), describes that one of the most efficient methods to control the output voltage gain is to incorporate a pulse width modulation (PWM) control in the inverters. He also mentions that the most used techniques are: single pulse width modulation, multiples, sinusoidal, modified sinusoidal, phase displacement [15]. Sine pulse width modulation is the most common[16], however there are others, such as: trapezoidal, stair, step, harmonic injection, delta, among others[15].

Sasi y Jisha (2013), mention that there are many PWM modulation schemes to obtain a variable voltage and frequency power supply. Of the PWM schemes they affirm that the most used are SPWM and SVPWM, but with the development of Digital Signal Processors (DSP) the SVPWM method has been more widely used for three-phase inverters because its implementation and linearity range is wide[19].

Mekhilev y Rahim (2002), developed a PWM modulation applied to a three-phase inverter with IGBTs using a Xilinx XC4008E FPGA. They use the technique of a sine wave generated through a lookup table or data stored in a programmable read-only memory (Erasable Programmable Read Only Memory (EPROM), the resolution depends on the data that represents the wave. Likewise, the triangle wave was performed by a counter from top to bottom, the count ratio determines the carrier frequency and the precision of the sampling process. For this case they used a carrier frequency of 18 KHz, the inverter's output frequency was set to 50Hz, this inverter was used with a grid-connected photovoltaic source[9].

Cortez (2008), describes the design of a trapezoidal PWM controlled three-phase inverter. To generate the PWM, it uses an integrated XR-2209, which is a timer connected to a 16F84 microcontroller, thus obtaining the desired frequencies. A 2 KHz carrier signal, it also uses three EEPROM memories, three analog-to-digital converters, and various amplifiers to cut, amplify, and match the signal. The results indicate that the output frequency varies from 53 to 96 Hz, output voltage of 80 to 160 Volts [2].

Osmanaj et al. (2010), show the theoretical analysis of the SPWM modulation applied to a three-phase inverter that feeds a 3 Horsepower (H.P.) motor, 380 V, 1725 revolutions per minute or rpm, the simulation was performed in Simulink from MatLab^{MR}. The frequency of the reference signal was 50Hz while the carrier signal was a 2 KHz triangle wave, corresponding to a modulation index of 40. The results show that the first harmonic was obtained around the carrier frequency of 1000 ± k * 50Hz, with a harmonic distortion of 4.1% [12].

Usama y Bilal (2015), present in their work a single-phase inverter controlled with a sinusoidal pulse width modulation, the output frequency for the inverter was from 5 to 50Hz, it was initially simulated in the Proteus^{MR} software and then implemented the SPWM algorithm in a microcontroller to control an inverter with IGBT transistors. In their conclusions describes that it can be improved using emerging technologies such as FPGAs and new DSPs, genetic algorithms and fuzzy logic [20].

Sadek et al. (2015), feature a Boost type CD/CD converter for variable impedance loading, using a PWM implemented in an FPGA and a PID control algorithm based on the converter transfer function in continuous time and converted to discrete time for implementation in VHDL. The PWM modulation has a frequency of 500 KHz, the FPGA is from the Spartan-3E family with 3S500 core. They also highlight the advantages of using an FPGA such as: parallelism, real-time work and high sample rates[18].

Patel y Raval (2015), simulated a three-phase inverter in MatLab^{MR}'s Simulink. For the trip of the inverter transistors, they generated an SPWM modulation, the control was in open loop, they worked an inverter without an output filter and another with a filter. The results of the waveforms show that the total harmonic distortion (TDH) of line voltage without filter was 84.98% and that of phase was 91.18%, with filter distortion improved to 2.33% and 3.18% respectively. It was then implemented with a microcontroller, a 16F series PIC protected with optocouplers. The result obtained in the construction was a total harmonic distortion of the output voltage of 30.74%, the inverter was made with the MOSFET IRF250N[13].

Adamu (2016), claims that the VHDL program can be considered as the description of the digital electronic system. In his work he implemented VHDL pulse width modulation on an FPGA to control a direct current motor. He first made a 5Hz, 5 KHz, and frequency divider module and made a 5-bit comparison module. So, with the comparison of a counter and a constant the result gave a single output PWM. It was implemented on the Xilinx^{MR} platform with a Spartan 3E card and ISE Project Navigator [1].

Based on the above, it can be said that different PWM algorithms have been developed for trip control of three-phase inverter transistors, to control the speed of motors, but these are sometimes complex and in many cases are subject to being strictly executed by the specific microprocessor or digital signal processor for which it was developed. Since, when programming is done, registers and output ports of those devices are included. Also, the algorithms that use the VHDL language to program an FPGA have several modules that generate sine and triangular signals using lookup tables, which makes them complex. Additionally, the algorithms are validated with the operation of the engine.

Based on the foregoing, this research proposes the statistical validation of a pulse width modulation algorithm or PWM based on a linear equation that allows controlling a three-phase inverter to vary the speed of an induction motor, in addition to which it can be programmed in any device.

II. METHODOLOGY

For the implementation and validation of the algorithm to control the inverter the following methodology was followed:

1. Design: a block diagram of the system to be implemented is formulated and each stage of the three-phase inverter is designed.
2. Based on the motor voltage specification, establish a linear equation that relates the pulse width and the desired output voltage of the reducing source.
3. From the motor specifications, the linear equation that relates the frequency variation and the pulse width is established.
4. An algorithm is designed to generate the PWM pulse width modulation with the linear equation.
5. Simulation of the designs of the different stages.
6. Construction of the reducing source and the three-phase inverter.
7. Implementation of the PWM algorithm in VHDL language and recording in the FPGA.
8. Carrying out tests and data analysis.
9. Validation of the algorithm.

2.1DEVELOPMENT

The system was proposed in a block diagram, as shown in Figure 2, the three-phase inverter was designed in MatLab[MR], it was immediately built, the supply was through a Buck switched source and both the source and the inverter were controlled by a FPGA applying pulse width modulation.

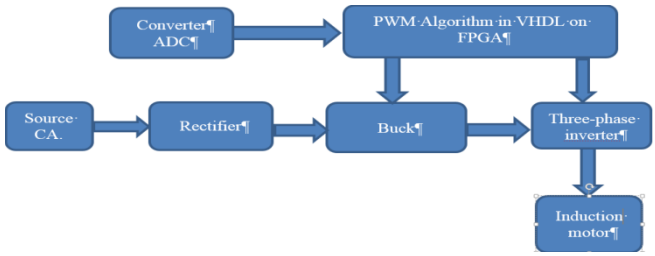

Figure 2. Block diagram of the three-phase inverter.

In particular, the module that generates the pulse width modulation algorithm through a linear equation is described. The technique was applied twice, once to control the output voltage of the reducing source, which in turn serves to supply the three-phase inverter, and once to control the output frequency of the three-phase inverter from a single input.

The PWM algorithm based on a linear equation was performed as follows:

- Determine the nominal values of the motor (voltage, frequency, speed).
- Determine the percentages of the above values, the maximums and minimums that you want to control. Set the maximum and minimum values of the control input (or set point).
- Detect the maximum count frequency (or count time) from the FPGA or microprocessor.
- Select the switching frequency.
- Divide the value of the maximum counting frequency by the switching frequency and obtain the value of the pulse width modulation output frequency counter.
- Obtain the duty cycle, through a rule of three between the switching frequency and the maximum and minimum value of the percentages previously calculated, two values are obtained.

- Relate the maximum and minimum value of the input (from the analog to digital converter) with the values calculated in the previous point.

According to Figure 2, a value initially is read from the Analog-Digital Converter (ADC) that is connected through the port called PMOD B of the Nexys 2 card, which consists of 8 inputs/outputs that are sufficient, since the ADC that was used is 8 bit.

In order for the frequency of the inverter to vary, the limits are required, that is, knowing the minimum and maximum frequency of the inverter output and second the frequency of the internal oscillator of the Nexys 2 card or the FPGA. Several manufacturers of frequency inverters and induction or alternating current (AC) motors do not recommend lowering the frequency below 20% of the nominal frecuency, as heating problems and loss of torque in the motor arise. In turn, they also recommend that the maximum frequency be only 10% above the nominal frequency.

As the three-phase induction motor that was used works at a nominal frequency of 50 Hz, 70 Volts and 1395 rpm, then the minimum frequency proposed in this work is 40 Hz and the maximum frequency is 55 Hz. To achieve this, the pulses that turn the inverter MOSFETs on and off must have a certain switching frequency.

Each branch or arm of the three-phase inverter (a, b, c) must have a frequency that goes from 40 Hz to 55 Hz and must be out of phase or displaced from each other 180^o. For this, each pulse must have a duration of 4.16 milliseconds for the minimum frequency and 3.03 milliseconds for the maximum.

The FPGA frequency is 50E6 and the desired PWM switching frequency is 25 KHz so the FPGA frequency/switching frequency ratio is made:

$$Counter_{25} = 50E^6 \text{ Hz}/25 \text{ KHz} = 2000$$

Taking equation 1 as a reference, the calculation of times to be fulfilled for the frequency variation is performed, taking $\alpha=60^o$ (because it is a three-phase six-step inverter) as follows:

$$\Delta t = \frac{\propto}{360 * f} [1]$$

Where:
α = Desired angle
f = Frequency in Hertz
Δt = Tripping time of transistors

With the time calculated for the minimum frequency and the clock time generated by the FPGA of 1 / 50E6 = .02µs, the lower counter = 4.16 ms / .02 µs = 208000 is obtained.

Likewise, the time for a maximum frequency and the FPGA clock time of .02µs, the upper counter = 3.03 ms /.02µs = 151500 is obtained.

These points make it possible to form an equation and graph it, as shown in Figure 3.

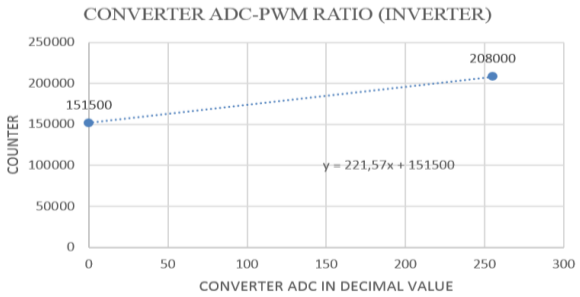

Figure 3. Ratio of the drive input and PWM for the three-phase inverter.

Another module of the main program is in charge of taking out a PWM signal that activates the transistor gate Q1 of the reducing source (Buck), which allows the variation of the supply voltage to the three-phase inverter.

This algorithm also begins with an ADC reading, since it controls the PWM duty cycle, which in turn controls the output voltage of the reducing source (Buck). Subsequently, the obtained reading must be converted into a decimal value to work with it.

Here too an equation is needed that relates the ADC input to the duty cycle value of the square signal. It is known that a 25 kHz signal and a duty cycle ranging from 30% to 80% of the power supply is required

which is 70 Volts, provided by the reducing source (Buck). Then the voltage that will supply the inverter can vary from 21 to 56 Volts.

With the above value and the nominal voltage of the three-phase motor of 70 Volts, the variation of the upper limit voltage of 80% is calculated to be equal to 56 Volts and a duty cycle of 1600 and the lower one of 30% which is equivalent to 21 Volts and 600 of duty cycle. The values of 1600 and 600 that correspond to the duty cycle were calculated from the switching frequency of the PWM whose value is 2000, with them the linear equation was obtained, as shown in Figure 4.

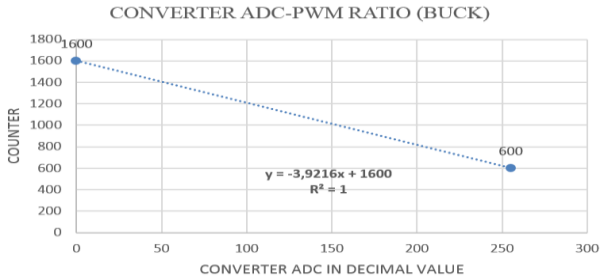

Figure 4. Value relation of the digital analog converter and the output frequency for the reducing source (Buck).

III. TESTS AND RESULTS

Measurements were made and 52 data were obtained from all the variables, as shown in Figure 5: frequency, inverter voltage and motor speed, measured from a minimum to a maximum of the digital analog converter. This to obtain the linear regression models that allow validating the algorithm. According to Landero (2014), to perform the linear regression, the assumption of data normality and variance homogeneity must be fulfilled [7]. Therefore, the SPSS^{MR} software was used to corroborate the characteristic of the values obtained from the measurements before marked.

	ADC VALUE	VOLTAGE	FREQUENCY	RPM
2	255	50	55	1561
3	250	47	54,6	1553
4	245	46	54,6	1546
5	240	45,5	54,5	1538
6	235	45	53,8	1532
7	230	44,2	53,4	1520
8	225	44	53,4	1516
9	220	43	52,9	1510
10	215	42,7	52,9	1501
11	210	42,4	52,3	1494
12	205	41,8	52	1486
13	200	41	51,9	1469
14	195	40,2	51	1471
15	190	41	51,3	1464
16	185	40,9	51	1457
17	180	40	50,8	1448
18	175	39,6	50,2	1441
19	170	39,2	49,7	1435
20	165	39	49,7	1426
21	160	38,4	49,4	1419
22	155	38	49	1412
23	150	37,2	48,9	1406

Figure 5. Values of measurements made.

The normality test was carried out through the Kolmogorov-Smirnov test because n is the number of measurements or data and is greater than 30. There is another test for normality also called Shapiro Wilk, the latter is used when the n data is less than 30 [7].

The hypotheses of the normality test are:

P_value => α Ho is accepted: the data comes from a normal distribution.
P_value<α H1 is accepted: The data does not come from a normal distribution.

Whereα is the level of significance.

According to the results of Table 1 obtained with SPSS^{MR}, it can be seen that the significance values are:

For the analog to digital conversion the P_value = 0.200, the voltage P_value = 0.200, for the frequency P_value = 0.200 and finally the dependent variable speed P_value = 0.200, all the values are greater than α = 0.05 so the null hypothesis is accepted Ho, all the independent and dependent variables have a normal distribution.

Table 1. Kolmogorov-Smirnov normality test for the measured variables.

Prueba de Normalidad de Kolmogorov-Smirnov

	Kolmogorov-Smirnov[a]			Shapiro-Wilk		
	Statistic	df	Sig.	Statistic	Df	Sig.
VOLTAJE MEDIDO	,095	52	,200*	,962	52	,092
VELOCIDAD MEDIDA	,067	52	,200*	,955	52	,050
FRECUENCIA MEDIDA	,105	52	,200*	,942	52	,013
CONVERSION ANALOGICA A DIGITAL	,064	52	,200*	,955	52	,050

The Homogeneity test of variance or equal variance (also called homoscedasticity), was carried out through the Levene test, highlighting that the number of data n is equal to 52 measurements. To do this test, all the measurements were grouped into four groups in a single variable called "measure variables" and the aforementioned test was applied to them, and the following hypotheses were established:

The hypotheses of the test of equal variances are:

P_value => α Ho is accepted: the data has equal variances.
P_value<α H1 is accepted: The data does not have equal variances.

Whereα is the level of significance.

According to the results of Table 2 obtained with SPSS[MR], it can be seen that the values of the Levene's statistic is 93,379 and the Pvalue of significance is .000, which is less than .05, so the null hypothesis is rejected and the alternative hypothesis is accepted, which means that the data has different variances, this assumption is not fulfilled. But according to Hildebrand (1999), this assumption is important if the sample sizes are substantially different and he mentions that when all the groups are equal in size, the effect of the highly unequal variances is minimal, in this case all the groups are 52 measurements [4]**.**

Table 2. Levene's test for homogeneity of variances of the measured variables.

Prueba de Levene homegeneidad de varianzas

		Levene Statistic	df1	df2	Sig.
VARIABLES_MEDIDAS	Based on Mean	93,379	3	204	,000
	Based on Median	93,379	3	204	,000
	Based on Median and with adjusted df	93,379	3	90,155	,000
	Based on trimmed mean	93,378	3	204	,000

After fulfilling the assumption of normality, a regression model was obtained between the values of the analog-digital converter and the frequency, as observed in the graph in Figure 6. This allows us to determine that the relationship of the converter with the width of the generated pulse by the algorithm put in the FPGA device it is linear, since the determination coefficient R^2 is almost unity. In the model, the dependent variable is "y" representing the output frequency and the dependent variable is "x" representing the value of the analog-digital converter.

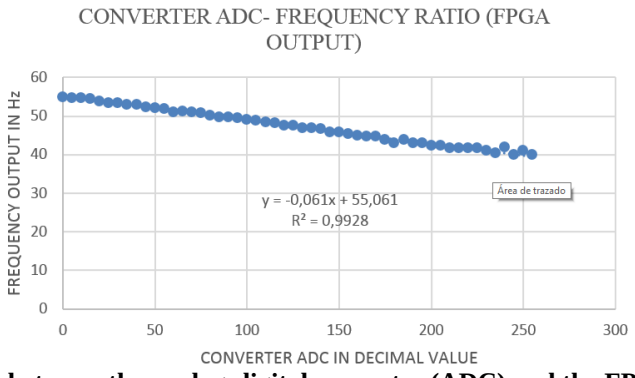

Figure 6. Relationship between the analog-digital converter (ADC) and the FPGA output frequency.

Likewise, the value of the inverter output frequency and the revolutions per minute of the motor were obtained, as shown in the graph in Figure 7. It can be verified that the motor varies its speed in the range of 40 Hz to 55Hz and with a speed of 1180 up to 1561 rpm respectively. Likewise, a linear regression model was obtained with a determination coefficient R^2 of 0.9925, which allows us to affirm that the model is valid in both cases. This mathematical model is shown in Figure 7. The dependent variable is the speed of the three-phase motor in revolutions per minute rpm identified in the equation by "y" and the independent variable is the frequency denoted in the equation by "x".

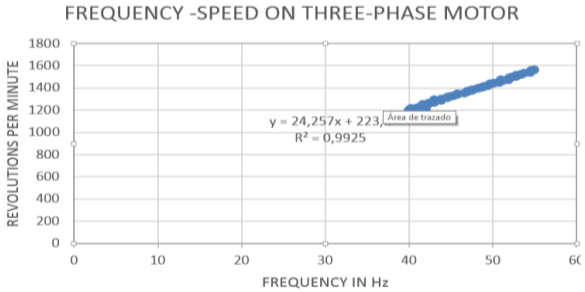

Figure 7. Relationship between FPGA output frequency and three-phase motor speed.

Because a motor varies its speed according to the supply voltage or frequency or both simultaneously, a model was also obtained for the relation between the analog-digital converter and the output voltage, which is supplied by the reducing source (Buck) to the three-phase inverter and this one to the motor. In Figure 8, the linear regression graph is shown with the mathematical model that relates the output voltage identified in the equation by “y” and the value of the analog-digital converter denoted by the letter “x” as a dependent variable and a factor of determination R^2 of 0.99 that allows us to say that the model is valid.

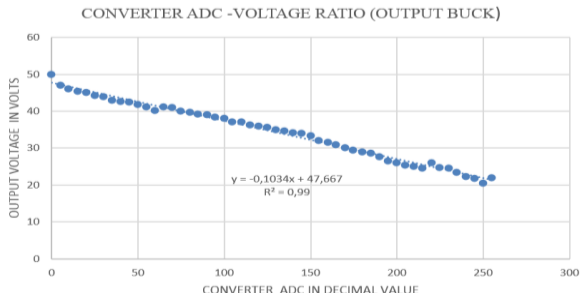

Figure 8. Relationship between the ADC converter and the source output voltage (Buck).

The inverter output voltage value and the revolutions per minute of the motor were measured, as shown in the graph in Figure 9. Identifying that the motor varies its speed in the range of 21 to 50 Volts, with a speed of 1180 to 1561 rpm respectively. A linear regression model was also obtained with a determination coefficient R^2 of 0.9903, which allows us to affirm that the model is valid. This mathematical model is shown in Figure 9. The dependent variable is the speed of the three-phase motor in revolutions per minute rpm identified in the equation by "y" and the independent variable is the voltage denoted in the equation by "x".

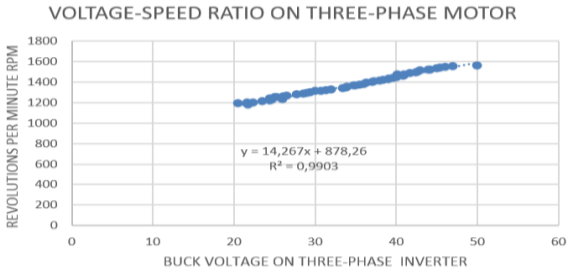

Figure 9. Relationship of source voltage (Buck) and motor speed.

Finally, the same process was performed with data directly from the converter and the motor speed, obtaining a linear regression model between both of them. In Figure 10, the graph and the mathematical model are shown, the dependent variable being the motor speed identified in the equation by "y" and the value of the

analog-digital converter as an independent variable denoted by "x" within the equation. The determination coefficient R^2 of 0.9998 can be identified, which indicates that the model is valid.

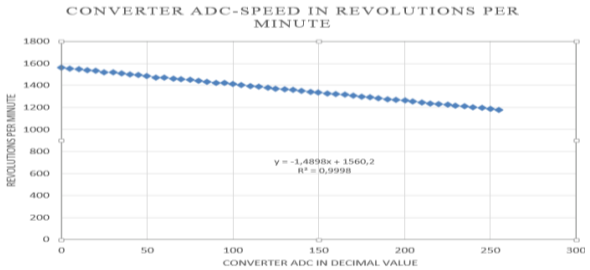

Figure 10. Ratio between the value of the converter and the motor speed in revolutions per minute.

IV. CONCLUSIONS

A PWM algorithm was developed using two linear equations, one to control the output frequency of the three-phase inverter and the other to control the voltage of the Buck reducing source.

The algorithm was programmed in the hardware description language on a programmable array of field gates. The outputs allow control of the pulse width to vary the voltage and frequency of a three-phase inverter. The algorithm presented here does not require complex calculations, nor does it generate tables of values of the modulating and carrier or reference wave.

The results obtained in this work are comparable to the reviewed literature. 52 measurements of frequency, voltage and speed were made, with them several graphs were generated where the linear regression models between the value of the analog-digital converter and voltage, the analog-digital converter and frequency are shown, in addition to the linear regression models between frequency, voltage and speed, show in all cases values close to 1 of the Pearson's coefficient and the determination coefficient R^2. This allows us to say that the models are valid and that according to the scatter diagram, the relationships are linear, implying that the algorithm works according to what was proposed.

REFERENCES

[1]. Adamu, M.M.U. (2016).“Digital system design with VHDL and FPGA controller based pulse width modulation”. International Journal of Electrical and Electronics Engineering Studies, Vol.3.
[2]. Cortez, C.D.J. and Conde, E.J. (2008).“Diseño de un inversor trifásico de voltaje con modulación ancho de pulso (PWM) trapezoidal”.Thesisin Ingeniería en Electrónica. Universidad Autónoma del Estado de México, Facultad de Ingeniería,Toluca:México, p.132.
[3]. Hart, D.W. (2001). “Power electronics”. McGraw-Hill Education.
[4]. Hildebrand, D.K. (1999). “Estadística aplicada a la administración ya la economía”.Adisson Wesley Iberoamericana.
[5]. Jimena, L.M.D., et al. (2007).“Modulación PWM aplicada a inversores trifásicos dentro del esquema de accionamientos eléctricos AC”. Universidad del Cauca, Facultad de Ingeniería Eléctrica y Telecomunicaciones (FIET).
[6]. Kaur, R. and Brar, G.S. (2016). “Induction motor drives-A literature review”. International Science Press, Vol.9, No.16, pp.8071-8081.
[7]. Landero, H.R. and González, R.M.T. (2014). “Estadística con SPSS y metodología de la investigación”. Editorial Trillas, México.
[8]. Mandujano, B.E.E. (2012). “Sinamics V20”. In Driver Sinamics V20. Siemens.
[9]. Melkhilev, S. and Rahim, N.A. (2002). ”XilinX FPGA based three-phase PWM inverter and its application for utility connected system”. Proceeedingof IEEE TENCON, pp.2079-2082.
[10]. Mohammed, S.A., Abdel-Moamen, M.A. and Hasanin, B. (2013). “A review of the state-of-the-art of power electronics for power system applications”. Quest Journal of Electronics and Communication Engineering Research (JECER), Vol.1, No.1, pp.43-52.
[11]. Mohan, N., et al. (2009). “Electrónica de potencia: convertidores, aplicaciones y diseño”. McGraw-Hill.
[12]. Osmanaj, S.F., Diellit, K.E., and Selimaj, R.A.(2010). “Control ofvoltagesourceinvertersusing SPWM strategyforadjustablespeedmotors”. Trends in the Development of Machinery and Associated Technology (TMT), pp.473-476.
[13]. Patel, J.A. and Raval, A.P.H.H. (2015). “Design of sinusoidal pulse width modulation inverter”.International Journal for Technological Research in Engineering, Vol.2, No.8.
[14]. Patiño, C.R., Torres, C.A. and Yarce, D.M. (2008). “Diseño y construcción de un inversor trifásico”. Scientia et Technica, Vol.3, No.40, pp.37-42.
[15]. Rashid, M.H. (2015). “Electrónica de potencia”. Pearson Educación, p.680.
[16]. Rojas, V.C.A. (2006). “Diseño y simulación de técnicas de modulación PWM natural para el control de motores de inducción trifásicos”. Facultad de Ingeniería y Arquitectura Programa de Ingeniería Electrónica,Pamplona:Colombia, pp.230-236.
[17]. Rosales, F., et al. (2009). “Implementación de un control V/Hz usando el MC3PHAC”. XIII Reunión de Trabajos en Procesamiento de la Información y Control, RPIC.
[18]. Sadek, U., et al. (2015). “FPGA-based control of a DC-DC boost converter”. IFAC-Papers OnLine, Vol.48, No.10, pp.22-27.
[19]. Sasi, D. and Jisha Kuruvilla, P. (2013). “Modelling and simulation of SVPWM inverter fed permanent magnet brushless dc motor drive”. International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol.2, No.5,pp.1947-1955.
[20]. Usama, H.S. and Bilal, A.H. (2015). “Speed and frequency control of AC induction motor using variable frequency drive”. Student Research papr Conference, pp.230-236.