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Effect OF Fin Height on electrical parameter of Tri-gate Junctionless FinFET

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Abstract
The non-planar 3D structure of Tri-gate Junctionless Finfet makes them able to be scaled down to 22nm and beyond and also have better performance. But variation of Fin height has an impact on the device performance. In this paper, the impact of various Fin Height on electrical parameter junctionless Tri-gate FinFET has been evaluated. Different important device electrical parameter such as ON current, OFF current, I_{ON}/I_{OFF}, Threshold voltage, Subthreshold slope, DIBL, Transconductance is evaluated for different Fin Height and analyzed. Results show that for long channel devices the better performance is obtained with higher Fin Height with higher I_{ON}/I_{OFF} and smaller values of Subthreshold slope, DIBL, whereas for short channel length devices better performance is found with smaller Fin Height due to reduced Subthreshold slope and DIBL and increased I_{ON}/I_{OFF} ratio. And To study the effect of the channel doping concentration on Tri-gate Junction less 22nm N- channel FinFET all the simulation are done on Visual TCAD software using Genius simulator.

Keywords: *Junction less FinFET, Visual TCAD, 22 nm Technology, DIBL, Subthreshold slope.*

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I. INTRODUCTION

In the family of FETs, FinFET provides better electrostatic control on the channel even in sub-nanometer dimensions. However, as the physical dimensions of the FinFETs are scaled down aggressively to a few nanometers, fabrication steps becomes too complex, as there is a need to produce a very shallow source and drain regions with high doping concentrations of the order of 10^{20} per cm^3. So, to overcome these problems, Junctionless FinFETs (JL-FinFETs) were developed. As Junctionless FinFET has no PN Junction in the source-channel-drain path, it can be scaled to lower channel length because of lower short channel effects and easy fabrication steps. It has homogeneous and uniform doping throughout the source-channel-drain region unlike a junction based FinFET.

1.1 **Device structure and simulation:** Fig.1 shows 2D cross-sectional view of Proposed Device and Fig.2 shows Schematic view of Proposed Device.

Fig.1 2D cross-sectional view of Proposed Device

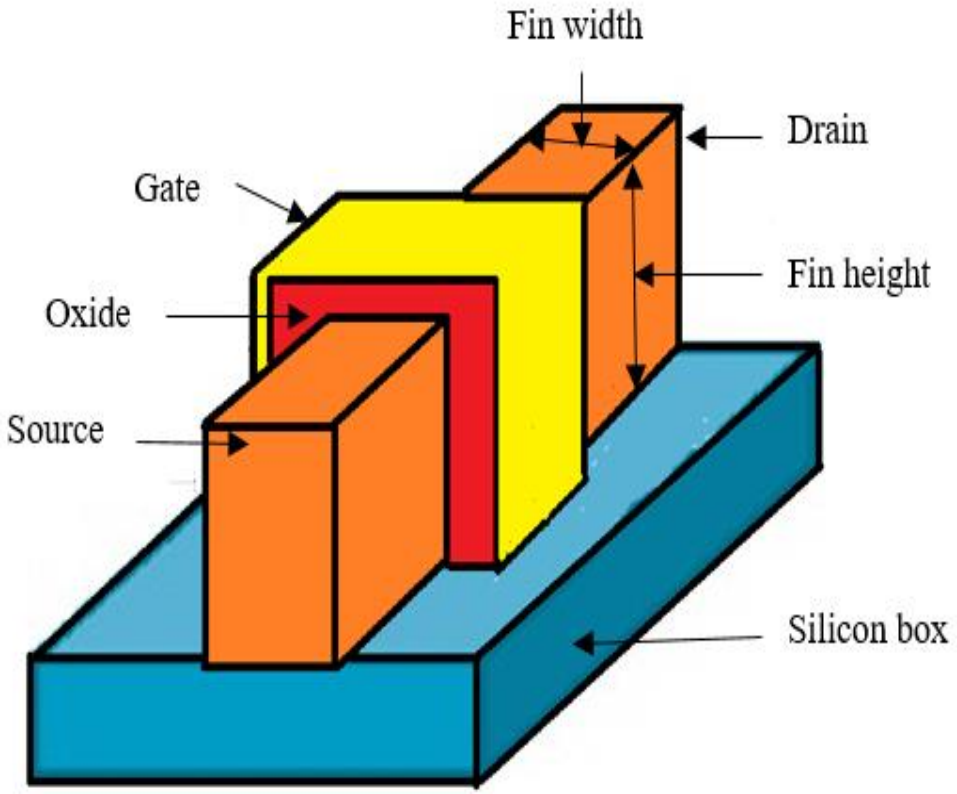

Fig.2 Schematic view of Proposed Device

Table: (a) Structure parameters of Proposed Device i.e. Dual Material Gate Trigate Junctionless 22nm FinFET

S. No	Parameter	Dimension
1.	Gate length	22nm
2.	Fin Height	10-20nm
3.	Fin Width	5nm
4.	Oxide Thickness	1nm
5.	Source, Channel & Drain Doping	1E19/cm^3
6.	Workfunction	5.2eV
7.	Gate oxide material	SiO_2

1.2 Electrical parameters of FinFET

a) Threshold voltage: It is the minimum gate to source voltage at which channel create between drain and source. It is define as the constant current threshold voltage. Threshold voltage is the gate to source voltage required to produce a drain current of 10E-7* Effective Width of Channel / Length of the gate.

Effective Width of Channel = $2H_{FIN} + W_{FIN}$ .....(1)

Where,

H_{FIN} = Height of FIN

W_{FIN} = Width of FIN

b) Subthreshold slope: It is define as the variation in gate voltage that has caused one decade increase in drain current.

$$SS = \frac{\partial V_{GS}}{\partial \log_{10} I_{DS}} \quad \text{.....(2)}$$

Where,

V_{GS} = Gate to Source Voltage

I_{DS} = Drain to Source Current

c) DIBL: In Ideal MOSFET drain current is controlled by gate but when the length of channel scale down, drain current is decreased by increasing drain voltage and this effect is commonly called DIBL.

$$DIBL = \frac{\partial V_{TH}}{\partial V_{DS}} \quad \text{.....(3)}$$

Where,

V_{DS} = Drain to Source Voltage

V_{TH} = Threshold Voltage

II. RESULT AND DISCUSSION

The results obtained are as discussed below

(i) I_{DS} ─ V_{GS} Transfer Characteristics for varying Fin Height

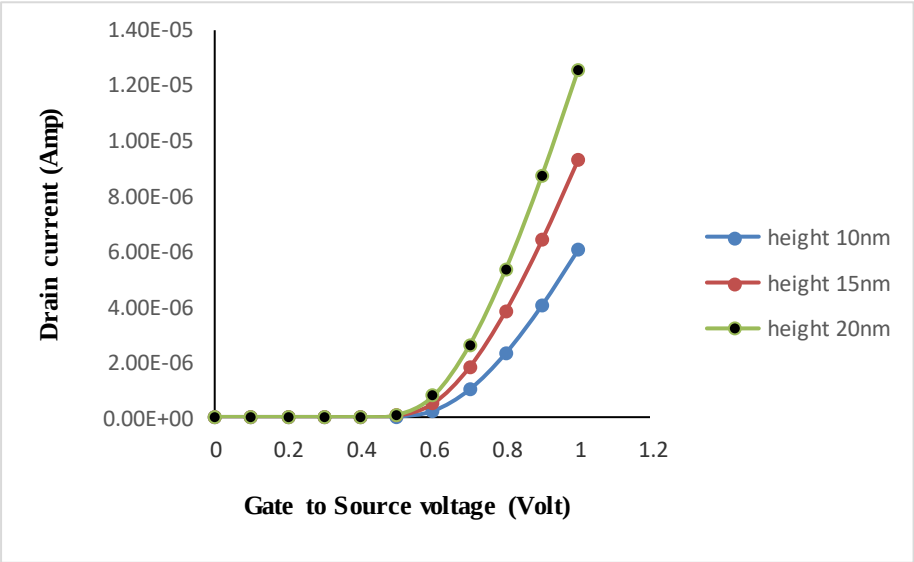

Fig.3: I_{DS} ─ V_{GS} Transfer Characteristics for varying Fin Height

I_{DS} ─ V_{GS} Transfer Characteristics for varying Fin height (10 to 20 nm) and source, channel & drain doping (10^19 /cm3) at V_D = 1V and V_{GS} ranging from 0 to 1V. From the I_{DS} ─ V_{GS} Transfer Characteristics as shown in Fig.3.

(ii) Effect of Fin Height on Leakage current

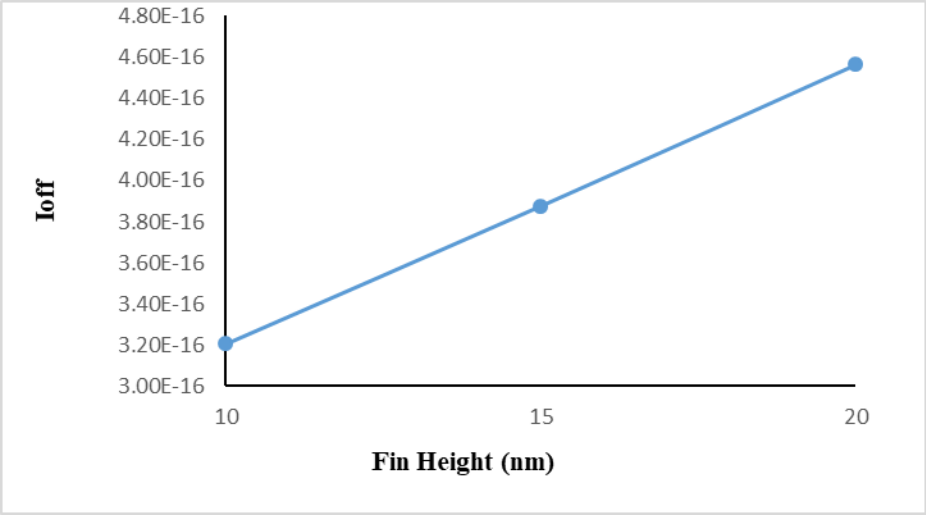

Fig.4: I_{OFF} of Proposed device for varying Fin Height

I_{OFF} of Proposed device for varying Fin height and source, channel & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.4. I_{OFF} increases with increasing Fin height because of gate supremacy over the channel.

(iii) **Effect of Fin Height on Drive Current**

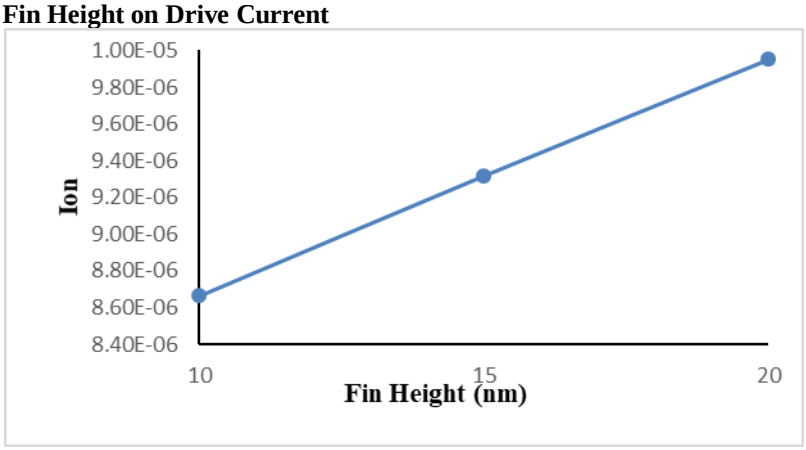

Fig.5: I_{ON} of Proposed device for varying Fin Height

I_{ON} of Proposed device for varying Fin height and source, channel & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.5. I_{ON} increases with increasing Fin height because of gate supremacy over the channel. The series resistance of the channel increases with reduction of Fin Height. Thus smaller Fin height, higher the channel's series resistance. As a result Drain current increases with increasing the Fin height. This leads to net increment in on current with the increasing the Fin Height.

(iv) Effect of Fin Height on Ion/Ioff ratio

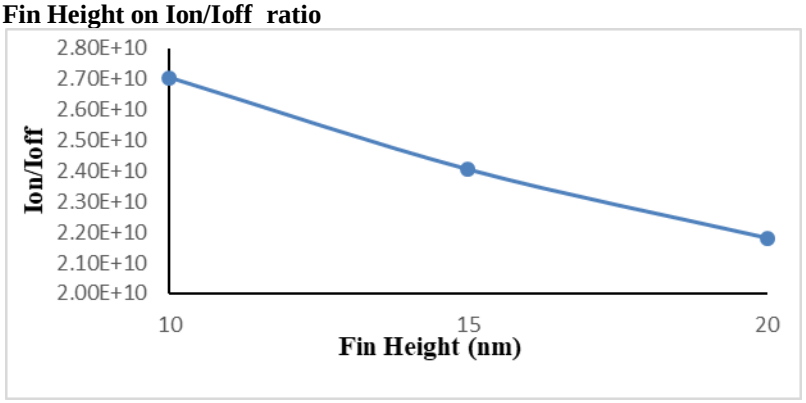

Fig.6: I_{ON}/I_{OFF} of Proposed device for varying Fin Height

I_{ON}/I_{OFF} of Proposed device for varying Fin height (10 to 20nm) and source, channel & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.6. I_{ON}/I_{OFF} decreases with increasing Fin height.

(v) Effect of Fin Height on Threshold Voltage

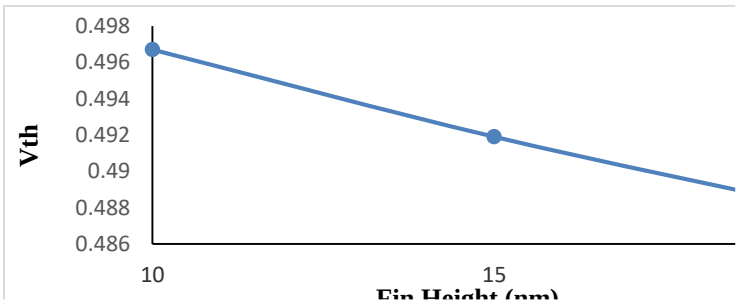

Fig.7: Threshold voltage of Proposed device for varying Fin Height

Threshold voltage of Proposed device for varying Fin height (10 to 20nm) and source, channel & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.7. Threshold voltage is weakly sensitive to Fin height. While for smaller Fin height the threshold increases due to the better electrostatic coupling of the gate in nano scale FinFET.

(vi) Effect of Fin Height on Subthreshold Slope

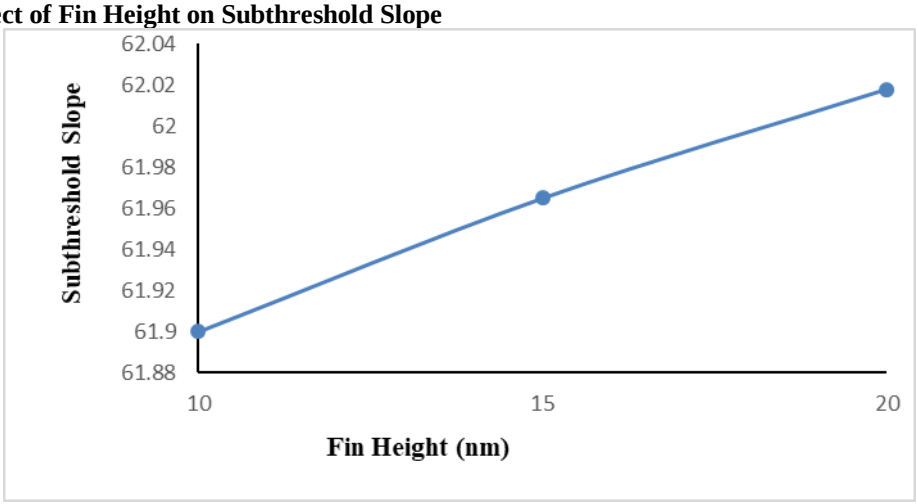

Fig.8: Subthreshold slope of Proposed device for varying Fin Height

Subthreshold slope of Proposed device for varying Fin height (10 to 20nm) and source, channel & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.8. For uniformly doped devices one, can see that for long channel devices (Lg = 100nm), the subthreshold slope shows low values, near ideal at 300k and especially at higher Fin height and as it decrease the subthreshold slope slightly increase. The opposite to the short channel devices (Lg = 22nm) with higher subthreshold slope overall values and the tendency to decrease SS as the Fin height decreases.

(vii) Effect of Fin Height on DIBL

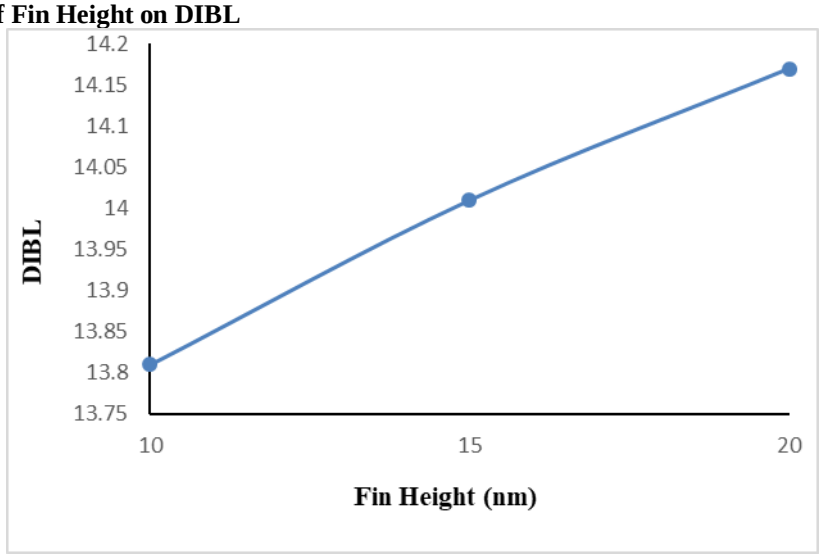

Fig.9: DIBL of Proposed device for varying Fin Height

DIBL of Proposed device for varying Fin height (10 to 20nm) and source, channel & drain doping (10^19 /cm3) at V_{DS} = 1V and V_{GS} ranging from 0 to 1V shown in Fig.9. With the Drain Induced Barrier Lowering (DIBL) the improvement on these devices comes from a smaller Fin Height. Long channel devices already have lower DIBL, and as the channel becomes shorter, the improvement of DIBL comes from lowering Fin height. This can be attributed to the strong electrostatic coupling of the gate on nanowire devices suppressing the short channel effects and decreasing the DIBL.

Table: (b) Comparison of Ioff current, Ion/Ioff, subthreshold swing, threshold Voltage and Drain Induced Barrier Lowering (DIBL) of proposed device with conventional FinFET.

S. No	Parameter	Proposed Device	Conventional FinFET
1.	I_{OFF}	3.21E-16	2.821e-10
2.	I_{ON} / I_{OFF}	2.70E+10	.621*(10^5)
3.	Subthreshold slope	61.9 mV/dec	70.0mV/dec
4.	DIBL	13.81 mV/V	50.0 mV/V

On comparing the Proposed device i.e. Tri-gate Junctionless 22nm FinFET with other devices i.e. conventional FinFET electrical characteristics ($I_{ON}/I_{OFF,}$ Subthreshold slope, DIBL) of proposed device has been significantly improved. Tri-gate Junctionless FinFET due to the presence of three gate, it provide better screening of short channel effects in term of DIBL, Subthreshold slope and improved ON state current, resulting in high I_{ON}/I_{OFF} ratio.

III. CONCLUSION

The dc characteristics Tri-gate JLFinFETs scaled down to 22nm channel length is investigated and the effects of varying the Fin height (10 to 20nm) is analyzed. It is observed that the threshold voltage decreases and ON-current decreases with increasing Fin height. DIBL and subthreshold swing of Tri-gate Junctionless devices are also measured and compared with that of conventional FinFET. A Tri-gate Junctionless FinFET has better control over channel charges, nearly ideal subthreshold slope, high ON/OFF current ratio, lower subthreshold leakage current. Thus JLFinFET is observed to suppress the short channel effects in a better way.

REFERENCES

[1]. A Cerdeira, B Iniguez, M Estrada. (2008) "Compact model for short channel symmetric doped double-gate MOSFETs" Solid-State Electronics, Vol. 52, Pp. 1064-1070.

[2]. J.P. Colinge, A. Kranti, R. Yan, C.W. Lee, I. Ferain, R. Yu, N. Dehdashti Akhavan, P. Razavi (2011) "Junctionless nanowire transistor (JNT): Properties and design guidelines" Solid-State Electronics, Vol. 65, Pp. 33-37.

[3]. Isabelle Ferain, Cynthia A. Colinge & Jean-Pierre Colinge (2011) "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors" Nature, Vol. 479, Pp. 310-316.

[4]. Chi-Woo Lee, Isabelle Ferain, Aryan Afzalian, Ran Yan, Nima Dehdashti Akhavan, Pedram Razavi, Jean-Pierre Colinge (2010) "Performance estimation of junctionless multigate transistors" Solid-State Electronics, Vol. *54*(2), Pp. 97-103.

[5]. R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn (2011) "Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm" IEEE electron device letters, Vol. 32, Pp. 1170-1172.

[6]. W. Rosner, E. Landgraf, J. Kretz, L. Dreeskomfeld, H. Schafer, M. Stadele, T. Schulz, F. Hofmann, R. J Luyken, M. Specht, J. Hartwich, W. Pamler, L. Risch (2004) "Nanoscale FinFETs for Low Power Applications" Solid-State Electronics, Vol. *48*, Pp. 1819-1823.

[7]. Ronald R. Troutman (1979) "VLSI Limitations from Drain-induced Barrier Lowering" IEEE Journal of Solid-State Circuits.

[8]. Gaurav Saini, Ashwani K Rana (2011) "Physical Scaling Limits of FinFET Structure: A Simulation Study" International Journal of VLSI design & Communication System, Vol.2, No.1.

[9]. T. A. Ribeiro and M. A. Pavanello, A. Cerdeira (2017) "Analysis of Bulk and Accumulation Mobilities in nand p-type Triple Gate Junctionless Nanowire Transistors" 32nd Symposium on Microelectronics Technology and Devices (SBMicro).

[10]. Antonio Cerdeiral, Fernando Avila Herrera, Bruna Cardoso Paz, Magali Estradal and Marcelo Antonio Pavanello (2015), "Role of the extensions in Double-Gate Junctionless MOSFETs in the drain current at high gate voltage" 30th Symposium on Microelectronics Technology and Devices.

[11]. Mukta Singh Parihar, Dipankar Ghosh, and Abhinav Kranti.(2013) "Ultra Low Power Junctionless MOSFETs for Subthreshold Logic Applications" IEEE Transactions on Electron Devices, Vol. No. 60.

[12]. Renan Trevisolii, Rodrigo T. Doriai, Michelly de Souzai and Marcelo A. Pavanellol (2015) "Effective Channel Length in Junctionless Nanowire Transistors" 30th Symposium on Microelectronics Technology and Devices.