International Journal of Research in Engineering and Science (IJRES)
ISSN (Online): 2320-9364, ISSN (Print): 2320-9356
www.ijres.org Volume 09 Issue 10 ǁ 2021 ǁ PP. 51-55

Implementation of Multiplier and Accumulator Unit Using Vedic Multiplier and Carry Save Adder

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ABSTRACT: *The Multiply-Accumulate Unit(MAC) is an integral computational component of all digital signal processing (DSP) architectures and thus has a significant impact on their speed and power dissipation and area overhead. To reduce the delay and area consumption the adders and multipliers and replaced with efficient adder and multiplier thereby implementing an efficient MAC unit. In this paper ,an efficient and high performance MAC unit is implemented using carry save adder and vedic multiplier for 32 bit operands. The proposed MAC unit has better area and delay compared to the existing MAC unit. The proposed method is synthesized and simulated using Xilinx vivado.*

KEYWORDS: MAC ,VHDL ,Carry save adder (CSA),DSP.

Date of Submission: 20-09-2021 Date of acceptance: 05-10-2021

I. INTRODUCTION

In recent years, Multipy -Accumulate unit(MAC) is developing for various high-performance applications. MAC unit is a fundamental block in the computing devices , especially Digital Signal Processing (DSP). MAC unit performs multiplication and accumulation process. Basic consistsmultiplier, adder and accumulator. MAC unit model is designed by incorporating the various multipliers such as Array Multiplier, Ripple carry Array Multiplier, Vedic Multiplier, Wallace Tree Multiplier and DADDA Multiplier in the multiplier module and the performance of MAC unit models is analyzed in terms of area, delay and power.

II. DESIGN OF MAC UNIT

In digital communication digital signal processer (DSP) is an important block which performs several digital signal processing applications such as convolution,Discrete cosine Transform (DCT),fourier Transform, and so on. Every digital signal processer contains MCA unit. The MAC unit performs bothmultiplication and accumulation processes repeatedly in order to perform continuous and complex operations in digital signal processing.MAC unit also contains clock and reset in order to control its operation. Many researchers have been focusing on the design of advance MAC unit architectures.

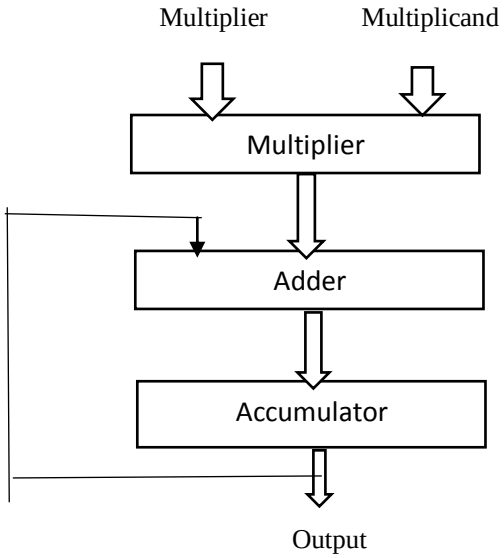


Figure 1: Block diagram of MAC unit

III. DESIGN OF ADDER ARCHITECTURE

Different adders that can be used for the design of a MAC unit are ripple carry adder, carry save adder and carry look ahead adder. The carry save adder seems to be the most useful adder for our application. It is simply a parallel ensemble of k full-adders without any horizontal connection. Its main function is to add three k-bit integer A,B,and C to produce two integers C' and such that C'+S=A+B+C. As an example,let A=40,B=25,and C=20,we compute S andC'as show below:

A = 40 =	1 0 1 0 0 0
B = 25 =	0 1 1 0 0 1
C = 20 =	0 1 0 1 0 0
S = 37 =	1 0 0 1 0 1
C' = 48 =	0 1 1 0 0 0

The i^th of the sum si and the (i+1)^st bit of the carry c'i+1 is calculated using the equations

Si = Ai + Bi+Ci

C'i+1 = AiBi + AiCi + BiCi

In other wortds a carry save adder cell is just a full-adder cell

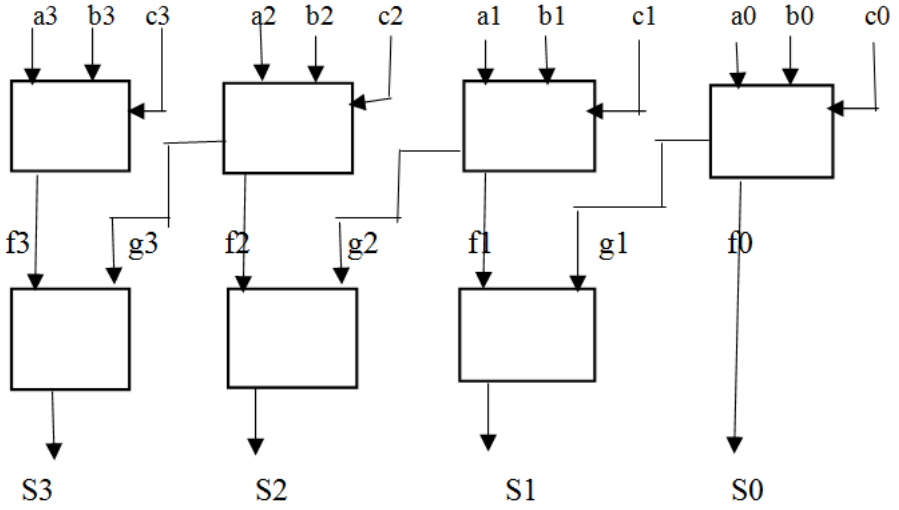


Figure2: Carry Save Adder

IV. DESIGN OF MULTIPLIER

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. Vedic mathematics is mainly word-formula which are termed as sutras. Vedic mathematics is the main given to the ancient system of mathematics or to be precise a unique technique of calculations based on simple rules and principles which main mathematical problems can be solved, be it arithmetic , algebra ,geometry or trigonometry. The system is based on vedic sutras or aphorisns,which are actually word formula describing natural ways of solving a whole range of mathematical problems.A simple digital multiplier (referred henceforth as vedic multiplier) architecture based on the urdhva thriyakbhvyam (vertically andcrosswise) sutra is presented. This sutra was traditionally used in ancient india for the multiplication of two decimal numbers in relatively less time.

V. RESULTS AND DISCUSSIONS

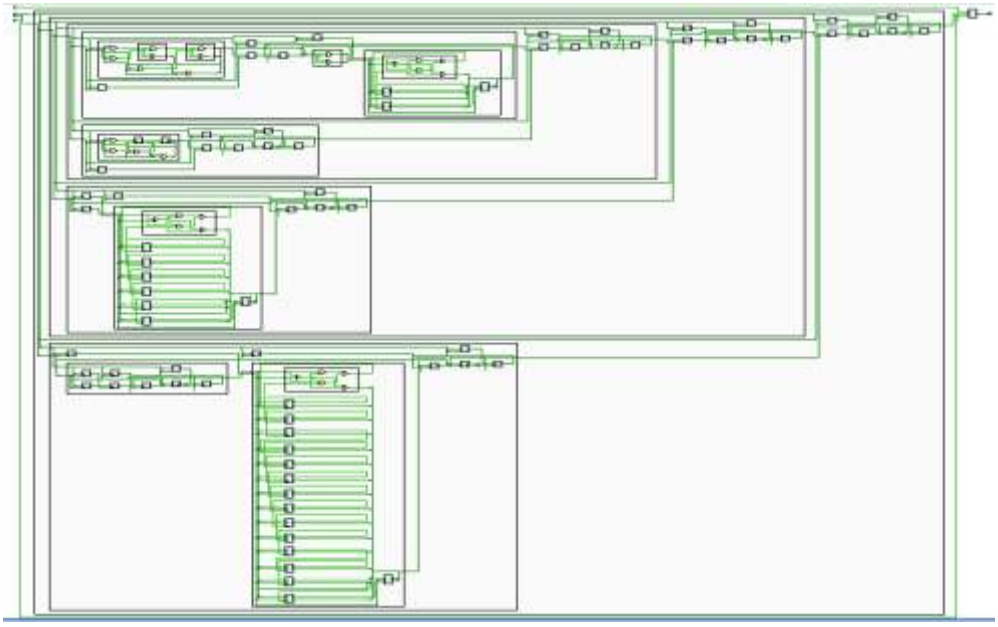


figure 2: RTL schematic of proposed MAC unit

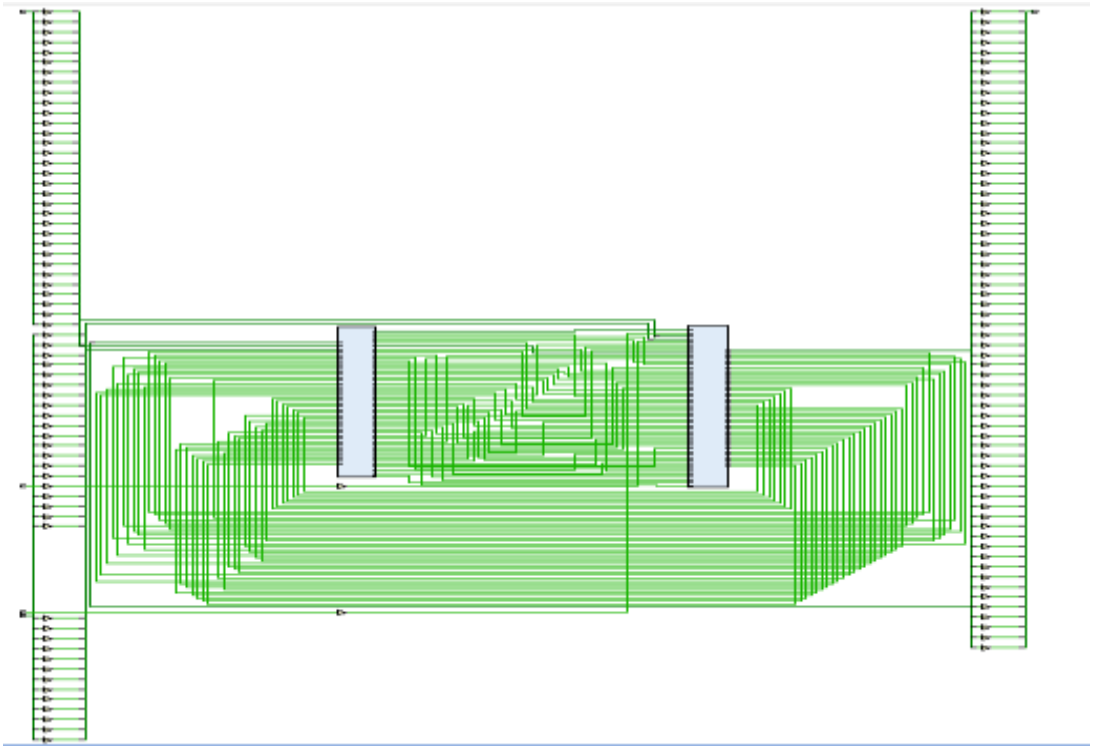


Figure 3: Technology schematic of MAC unit

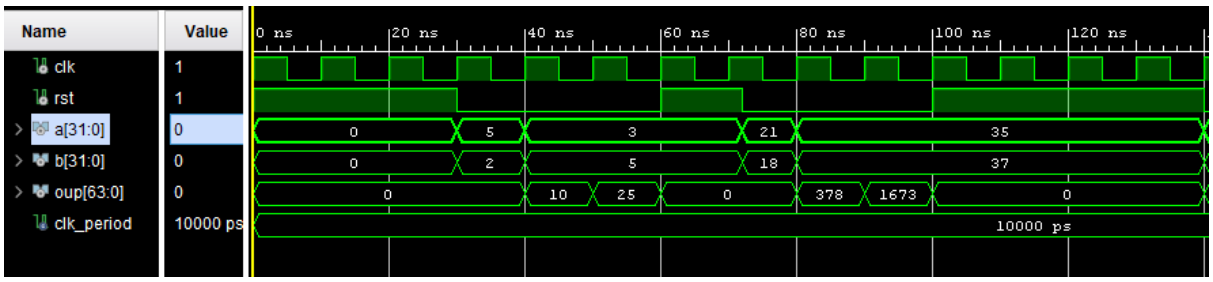


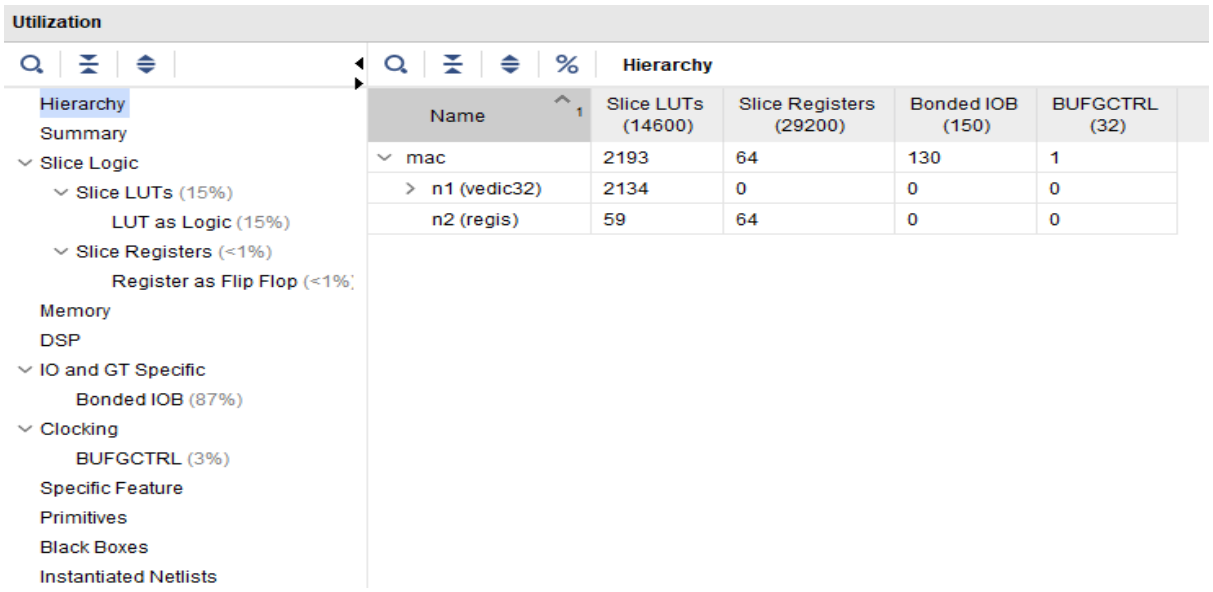
Figure 4 :Simulation result

Delay report:

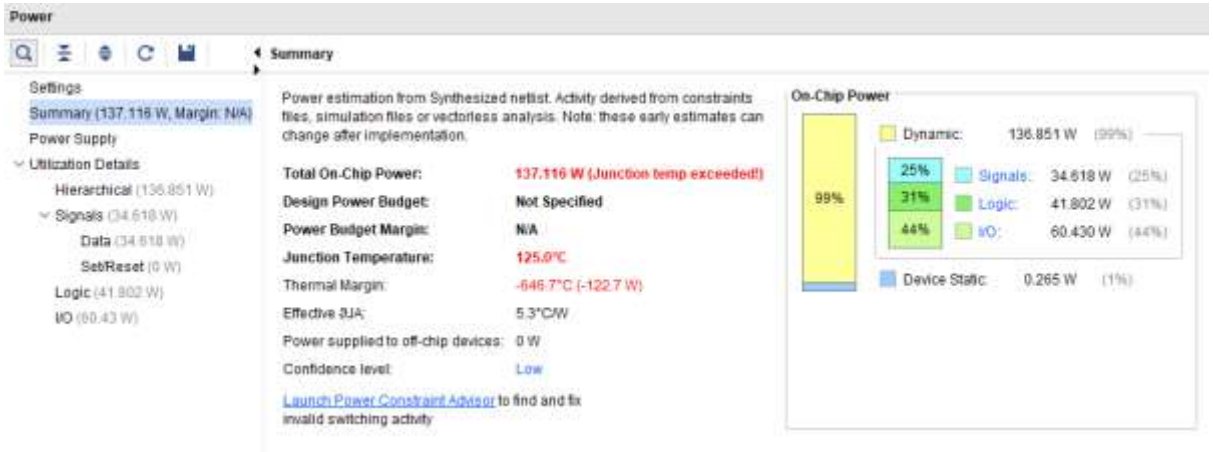
```
Timing Report

Slack:                  inf
  Source:               b[11]
                          (input port)
  Destination:          n2/oup_reg[63]/D
  Path Group:           (none)
  Path Type:            Max at Slow Process Corner
  Data Path Delay:      22.052ns  (logic 4.257ns (19.303%)  route 17.796ns (80.697%))
  Logic Levels:         33  (IBUF=1 LUT2=1 LUT3=2 LUT4=2 LUT5=3 LUT6=24)
```

Area report:



Power report:



Evaluation table for area, delay & power:

	Area (LUT)	Delay(ns)	Power(w)
Proposed Mac unit	2193	22.052	137.116

VI. CONCLUSION

In this paper, we proposed a better adder and multiplier replacing the existing circuits that are used to design MAC unit which can be efficiently utilized to trade of power and delay and area over ahead our approach aimed to reduced delay of a conventional mac unit by replacing the multiplier and adder with vedic and CSA respectively synthesis and simulation results show that the proposed multipliers show better performance in terms of area delay and power by modifying the adder and multiplier architectures, we can achieve better results in terms of area.

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