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Design and Simulation of 15 Level Cascaded H-Bridges Multi Level Inverter with SPWM and SVPWM Techenique and LCL Filter for Harmonic Reduction

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Abstract
This paper aims to determine the design simulation and implementation of a 15-level Cascaded H-Bridge (CHB) Inverter using Space Vector Modulation (SVM) and compares its performance with Sinusoidal Pulse Width Modulation (SPWM). The paper presents mathematical modeling, simulation analysis, and performance evaluation using MATLAB/Simulink. A comparative study of SPWM and SVPWM is conducted to evaluate their impact on harmonic distortion, efficiency, and switching losses. The results validate the improved waveform quality and efficiency of the proposed system, making it a promising solution for industrial and renewable energy applications.
Keywords: *Cascaded H-Bridge Inverter, Space Vector Modulation, Sinusoidal PWM, Multilevel Inverter, Harmonic Reduction, MATLAB Simulation, Power Electronics.*

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I. INTRODUCTION

Power electronics have revolutionized modern electrical systems, with inverters crucial in energy conversion applications. Among different inverter types, multilevel inverters (MLIs) have gained prominence due to their ability to generate high-quality output waveforms with reduced harmonic distortion and lower switching losses. MLIs are widely used in renewable energy systems, motor drives, and power transmission due to their enhanced efficiency and modular structure. This paper focuses on the 15-level Cascaded H-Bridge (CHB) inverter and explores its performance using Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Modulation (SVM) techniques.

Traditional H-bridge inverters have been extensively used in industrial applications due to their simple switch configuration and ease of control. However, their output contains significant harmonic distortion, making them unsuitable for high-performance applications. Pulse Width Modulated (PWM) inverters operating at high switching frequencies offer better output quality but suffer from high switching losses and electromagnetic interference (EMI) issues. These limitations have led to the adoption of Multilevel Inverter (MLI) topologies, which generate stepped voltage waveforms that improve power quality and system efficiency.

Need for multilevel inverters.

Multilevel inverters have been introduced to overcome the shortcomings of traditional two-level inverters, which must switch between two extreme levels of DC-link voltages. This results in:

- Higher harmonic content in the output voltage.
- Increased dv/dt stress on power semiconductor devices, affecting their longevity.
- Significant switching losses at high power levels, make PWM-based voltage source inverters (VSIs) inefficient for industrial applications.
- Electromagnetic interference (EMI) issues, which complicate the design of power circuits

Multilevel inverters address these challenges by generating multiple voltage levels, significantly reducing harmonic content and switching losses while ensuring smoother waveform transitions.

Advantages of Multi-Level Inverters

Multilevel inverters provide several advantages over conventional inverters, including:

- Reduced Total Harmonic Distortion (THD), improving power quality.

- Lower switching losses, leading to improved efficiency.
- Better voltage sharing, enabling the use of low-rated power devices in high-voltage applications.

This study focuses on the design and implementation of a 15-level Cascaded H-Bridge (CHB) Inverter with Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Modulation (SVM) techniques. The paper evaluates harmonic distortion, efficiency, and switching performance, providing a comparative analysis of these modulation techniques.

Several studies have demonstrated the advantages of MLIs over conventional inverters. Research highlights that SPWM and SVPWM significantly impact THD, efficiency, and DC bus utilization. While SPWM remains a widely adopted modulation technique for its simplicity, SVPWM offers improved voltage utilization and lower harmonic distortion, making it a superior alternative for high-power applications.

Recent advancements in MLIs include hybrid modulation techniques and artificial intelligence-based control strategies for further efficiency enhancement. Researchers have proposed optimized switching algorithms that minimize losses and enhance output waveform quality. Additionally, the integration of MLIs with renewable energy sources, such as solar and wind power, has gained traction due to their ability to handle fluctuating power levels effectively. Studies also suggest that adopting wide-band gap semiconductor devices, such as SiC and GaN, further improves the efficiency and power density of MLIs. Other studies have explored the impact of novel topologies like packed U-Cell and cascaded asymmetrical configurations in achieving better performance in terms of cost and efficiency.

II. System Design and Methodology

In Sinusoidal Pulse Width Modulation (SPWM), the switching table determines the gate signals for the inverter switches by comparing a sinusoidal reference signal with a high-frequency triangular carrier wave. When the sinusoidal reference is higher than the carrier wave, the switch is turned ON; otherwise, it remains OFF. The table follows a predefined pattern to generate symmetrical pulses, ensuring a smooth sinusoidal output. Proper selection of switching states helps in minimizing harmonics, improving power quality, and maintaining efficient voltage control in the inverter system.

Table: 1 Switching table for the proposed model

Voltage Level (V)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28
7	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
6	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1
5	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
4	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1
3	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
-2	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
-3	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
-4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0
-5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
-6	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0
-7	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

In a 15-level inverter, Space Vector Pulse Width Modulation (SVPWM) works similarly to a basic single-phase inverter but with more voltage levels, creating a much smoother AC output. Unlike a simple inverter that switches between just +Vdc, 0V, and -Vdc, a 15-level inverter has multiple intermediate voltage steps, reducing harmonics and improving efficiency. The goal is to generate a nearly sinusoidal waveform while making the best use of the available DC voltage.

Here's how the switching states work:

- Highest Positive Voltage (+Vdc): The load is fully connected to the positive side of the DC bus.
- Intermediate Voltage Levels (+13Vdc/14, +11Vdc/14, etc.): The inverter gradually steps down the voltage, creating a smoother transition.
- Zero State (0V): The load is momentarily shorted to balance the switching and reduce unwanted harmonics.
- Intermediate Negative Levels (-11Vdc/14, -13Vdc/14, etc.): The voltage gradually moves toward the negative side.
- Highest Negative Voltage (-Vdc): The load is fully connected to the negative DC bus.

By carefully modulating these switching states, SVPWM ensures efficient operation, reduced harmonic distortion, and better voltage utilization, making 15-level inverters ideal for high-power applications like renewable energy and industrial drives.

In a Cascaded H-Bridge (CHB) inverter, multiple H-bridge inverters are connected in series to generate a stepped AC output with higher voltage levels. For SPWM (Sinusoidal Pulse Width Modulation) in CHB, each H-bridge unit receives a sinusoidal reference signal phase-shifted accordingly and compared with a high-frequency carrier wave. This technique ensures smoother voltage transitions, reducing harmonics.
For SVPWM (Space Vector Pulse Width Modulation) in CHB, the switching states are selected based on space vector principles, optimizing the DC bus voltage utilization. By effectively combining switching vectors, the CHB inverter achieves better harmonic performance, efficiency, and reduced voltage stress on the switches.

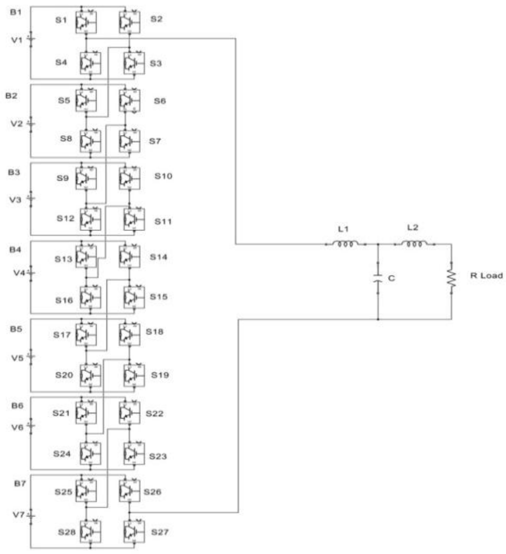

Figure 1 Purposed circuit diagram

Filter Circuits

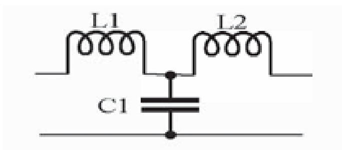

Figure 2 proposed LCL filter.

The Values of all the inductors L1 and L2 are the same and Given by

$$L=\frac{Z}{2\pi fc}$$

Where L1 and L2 are equal to L, Z equals the Load impendence at the filter Load Side and Fc is the cut-off frequency the Capacitance value can be found from an equation from the paper LCL design and be modified as

$$C=\frac{2}{Lwc2}$$

$W_c=2\pi f_c$ The capacitor C1 is equal to C of the equation

Table 2 LCL Filter values

Components	Values
Inverter-side Inductor (L1)	0.421 mH
Grid-side Inductor (L2)	0.210 mH
Filter Capacitor (C)	150.43 nF

Simulation and Results

The simulation of the Cascaded H-Bridge (CHB) inverter using SPWM and SVPWM techniques models the generation of multi-level AC waveforms. It demonstrates switching control strategies, voltage levels, and harmonic performance under different modulation techniques. The results help analyze THD (Total Harmonic Distortion), switching losses, and system efficiency.

Table 3: specifications of the PWM Technique

Parameter	Value
Carrier Frequency (f_c)	50 kHz
Modulating Frequency (f_m)	50 Hz
Modulation Index (M)	0.706
Frequency Ratio (f_r)	1000

Switches	28 switches
DC Sources	7 DC sources (each 46.42V)
No. of Levels (N)	15-level

III. Simulation Circuit and Waveform

The Cascaded H-Bridge (CHB) inverter operates with a 15-level output, utilizing 7 DC sources of 46.42V each and 28 switches for proper modulation. A 50 kHz carrier frequency and 50 Hz modulating frequency result in a frequency ratio of 1000, ensuring smooth waveform synthesis. The modulation index of 0.706 optimizes the inverter's performance, balancing harmonic reduction and voltage utilization.

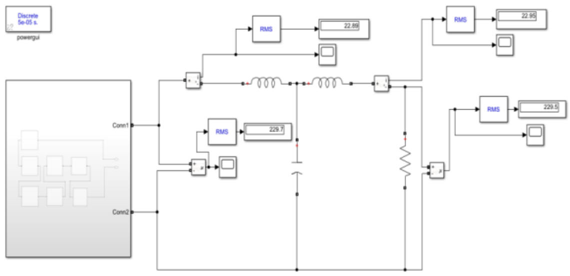

Figure 2 Matlab Simulink circuit diagram of the model

This simulation circuit diagram represents the implementation of both SPWM and SVPWM control techniques for a single-phase15 Level Cascaded H Bridge multilevel inverter. The system includes RMS voltage measurement blocks to monitor output voltage and current at different points. The power circuit consists of an H-bridge inverter, an LCL filter, and a load, ensuring smooth AC output with minimal harmonics.

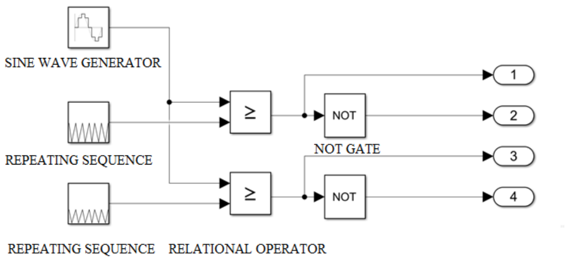

Figure 3 matlab-simulink model for parent signal generation

This control circuit implements Sinusoidal Pulse Width Modulation (SPWM) by comparing a sine wave reference with a high-frequency carrier signal using relational operators. The outputs control the switching states of the inverter, with NOT gates generating complementary signals. This ensures balanced switching and efficient AC waveform generation.

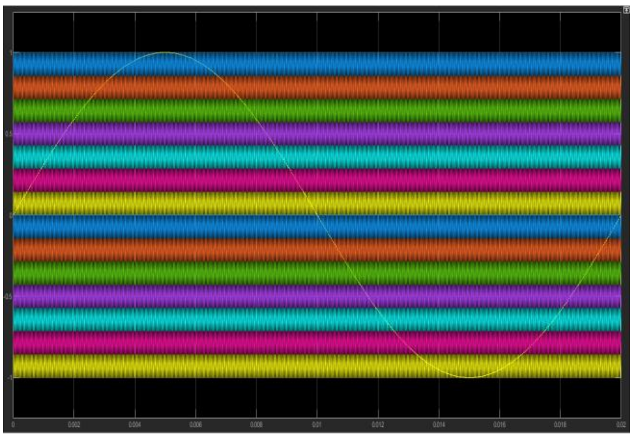

Figure 4 Parent Signal

This signal plot represents Sinusoidal Pulse Width Modulation (SPWM), where a reference sine wave (yellow) is compared with multiple high-frequency carrier waves. The modulated output switches between states, producing distinct pulse patterns (color bands) corresponding to different inverter switching signals. This method ensures efficient AC waveform generation with minimal harmonics.
Using MATLAB/SIMULINK software, the H-bridge inverter is simulated without having an LCL filter. Also, the 15-level filter is simulated without the proposed passive LCL filter. Fig 5 shows the output voltage of the H-bridge inverter without any filter and SPWM and SVPWM switching consecutively.

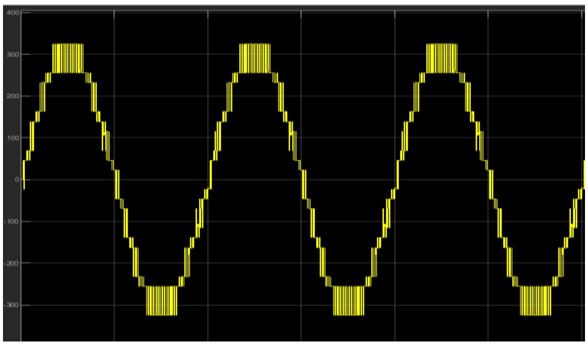

Figure 5 Output of inverter 15 level

IV. Result and Analysis

The harmonic spectrum analysis and Total Harmonic Distortion (THD) of the output voltages of the H-bridge inverter having SPWM and SVPWM switching and the 15-level inverter are shown in Fig. 6

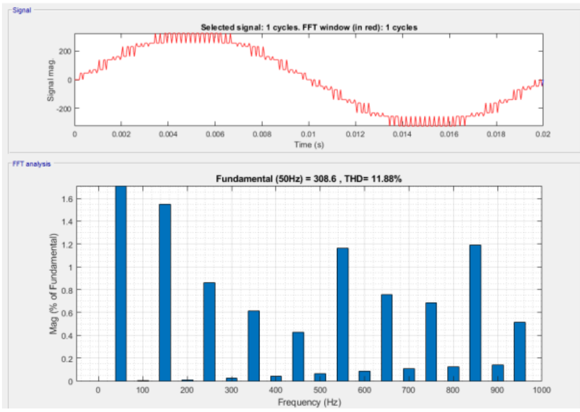

Figure 6 outputs of 15 levels CHB MLI without filter

Fig 6 shows a modulated signal over one cycle, likely from an SPWM inverter. The bottom FFT analysis indicates a fundamental frequency of 50 Hz with a Total Harmonic Distortion (THD) of 11.88%, showing harmonic components at multiples of 50 Hz. The presence of harmonics suggests some waveform distortion, which can impact power quality.

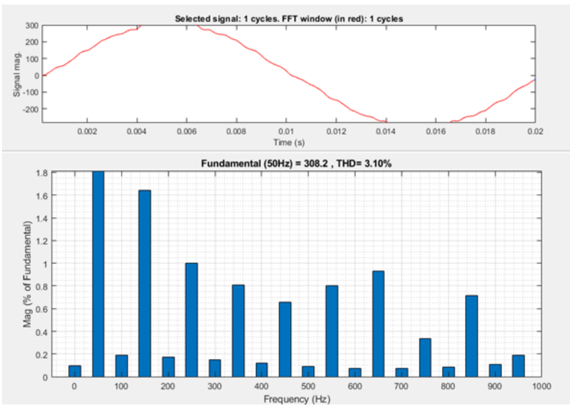

Figure 7 after LCL filter for SPWM

Fig 7 shows a modulated signal over one cycle, likely from an SPWM inverter after the filter. The bottom FFT analysis indicates a fundamental frequency of 50 Hz with a Total Harmonic Distortion (THD) of 3.10%, showing harmonic components at multiples of 50 Hz. The presence of harmonics suggests some waveform distortion, but it is ok for the power usage.
The Harmonic spectrum analysis and Total Harmonic Distortion (THD) of the output voltages of the H-bridge inverter having SPWM switching and the 15-level inverter are shown in Fig. 6

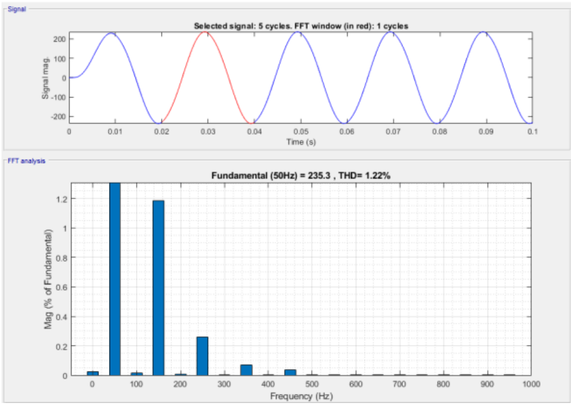

Figure 6 Harmonic Spectrum analysis

Table *4* presents the output values for different load resistances (R) in two cases: (a) and (b), both with and without a filter. In case (a), the output without a filter remains nearly constant across varying load resistances, ranging from 11.84V to 11.88V. However, with the filter, the output voltage is significantly reduced, ranging from 3.2V to 4.54V, with a slight increase at higher resistances. In case (b), the output voltage without a filter shows a wider variation, increasing from 11.96V at 50Ω to 22.14V at 200Ω. With the filter, the voltage remains much lower, ranging from 1.01V to 2.07V. The results indicate that the filter significantly reduces voltage levels across the load, and its impact varies based on resistance values. These findings highlight the influence of filtering on voltage regulation in different load conditions.

Table 4 (a) filter values with SPWM Technique (b) filter values with SVPWM Technique

R Load		
R Ω	Without filter	With Filter
10 Ω	11.84	3.36
20 Ω	11.88	3.2
50 Ω	11.88	4.01
100 Ω	11.88	4.54
200 Ω	11.88	4.49

(b)

R Load		
R Ω	Without filter	With Filter
10 Ω	13.03	1.22
20 Ω	12.66	1.16
50 Ω	11.96	1.01
100 Ω	15.48	1.32
200 Ω	22.14	2.07

Comparative Analysis of SPWM and SVPWM

Parameter	SPWM	SVPWM
THD (%)	Higher	Lower
Switching Losses	Higher	Lower

DC Bus Utilization	Moderate	Improved
Computational Complexity	Low	Higher

V. CONCLUSION

Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are two widely used techniques for controlling inverters, especially in motor drives and power electronics applications. SPWM works by comparing a sinusoidal reference signal with a high-frequency triangular carrier wave to generate switching pulses. It's relatively simple to implement but has some limitations, such as lower voltage utilization (only about 78.5% of the DC bus voltage) and higher harmonic distortion, which can lead to inefficiencies in performance.

On the other hand, SVPWM takes a more advanced approach by using space vector representation to optimize switching sequences. This method increases voltage utilization up to 86.6%, reduces harmonic distortion, and improves efficiency. Because of this, SVPWM is commonly used in high-performance applications like industrial motor drives and electric vehicles. However, it is more complex to implement compared to SPWM since it requires coordinate transformations and precise sector identification.

It depends on the application. If you're working on a basic inverter or a lower-power system, SPWM is easier and gets the job done. But if you need better efficiency, lower losses, and improved voltage utilization—especially for industrial and high-power applications—SVPWM is the smarter choice. If your project involves a 15-level Cascaded H-Bridge Inverter, SVPWM would be a better fit for achieving optimal performance.

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