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Resilient Symmetrical 8T SRAM cell for Leakage Power Attack using90nm CMOS Technology

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Abstract - *Static Random Access Memory (SRAM) occupies an important role as a memory device in VLSI circuits due to its storage capacity. SRAM is widely used as computer's cache memory and it gives low power consumption. Side channel attack due to leakage power has become a serious threat to security systems, as it enables secret (personal) data extraction. To provide resiliency to these types of attacks, we propose a symmetric 8T SRAM cell. The design of 8T SRAM cell is carried out using 90nm CMOS technology with the help of cadence virtuoso tool. In this paper 8T SRAM cell is compared with conventional 6T SRAM cell which provides less leakage power. The performance analysis of 6T SRAM and 8T SRAM with respect to delay analysis, power dissipation and leakagepower analysis observed and compared.*

Key Words: SRAM, VLSI, CMOS, Delay, Power dissipation,leakage power.

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I. SRAM

Static random access memory (SRAM) is a static memory cell which uses filpflop's to store each bit of data. It is widely used in various electronic systems. The data in SRAM memory does not require periodic refreshing. It is faster and consumes less power as compared to other memory cells. Because of this, SRAM is the most popular memory cell among VLSI designers.

SRAM operations

Conventional 6T SRAM cell consist of two inverters connected back to back. The output of the first inverter is connected to the input of the second inverter and vice versa. Basically, SRAM performs three operations which are Hold,Read and Write operations.

Hold operation: In standby operation or hold operation the word line (WL) is in off state. Access transistors connectedto the word line and B & BLB lines are also in off state.

For SRAM to operate in read or write mode the word line should always be high.

Write operation: The process of storing a data is known as write operation. It is used for uploading the contents in a SRAM cell. Write operation starts with assigning the values to be written at the Bit and its complimentary value at Bit'. In order to write '1' Bit is pre-charged with high voltage and the complimentary value '0' is assigned to Bit'. When M5 and M6 are set in ON condition by asserting WL 'high', the values assigned at Bit gets stored in the latch as Data. The M5 and M6 MOS Transistors are designed to be much stronger than the relatively weak transistors in the cell Ml, M2, M3 and M4 so that they are able to override the previous state of the cross-coupled inverters.

Read operation: The process of recovering the data is known as Read operation. It is used for fetching the contents. The Read Operation is started by asserting the word line 'WL' high which enables both the access transistors M5 andM6 after pre-charging both the Bit and Bit' lines to a logical

1. The second step occurs when the values stored in Data and Data' are transferred to the Bit lines by leaving Bit at itspre-charged value and discharging Bit' through M4 and M6to logical 0.

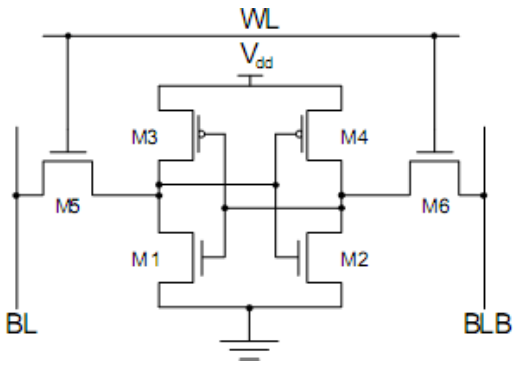

Fig 1: Conventional 6T SRAM

CMOS

Complementary metal–oxide semiconductor (CMOS) technology is used for constructing integrated circuit (IC) chips, including microprocessors, microcontrollers, memory chips (including CMOS BIOS), and other digital logic circuits. In CMOS both N-type and P-type transistors are used to design logic functions. The 2 important characteristics of CMOS devices are high noise immunity and low static power consumption. These characteristics allow CMOS to integratehigh density of logic function on a single chip.

Side-channel attack

Side channel attack is a type of attack in which the attacker tries to extract the secret data by using the unintended side channel leakage information. Side channel leakage may include timing information, power dissipation, EMF (electromagnetic fields).

Leakage power

Leakage power is the unwanted sub-threshold current in thetransistor even when the transistor in OFF mode.

Leakage power attack

Leakage power attack is the security exploit that attempts toextract secret data from a chip or a system.

II. Design

6T SRAM in 90nm CMOS technology

The design of 6T SRAM in 90nm CMOS technology is done using Cadence tool. The schematic consist of word line(w),input (b, b') and output (q, q').

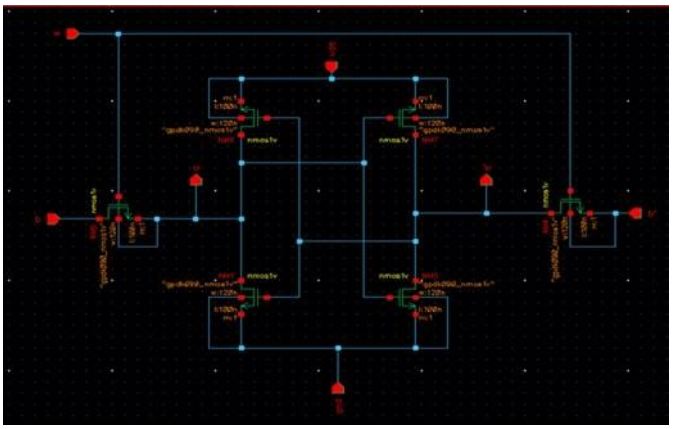

Fig 2 : Schematic of 6T SRAM

In test bench, we have given the supply voltage (Vdc) as1.8v and input lower to higher voltages as 0v to 1.8v.

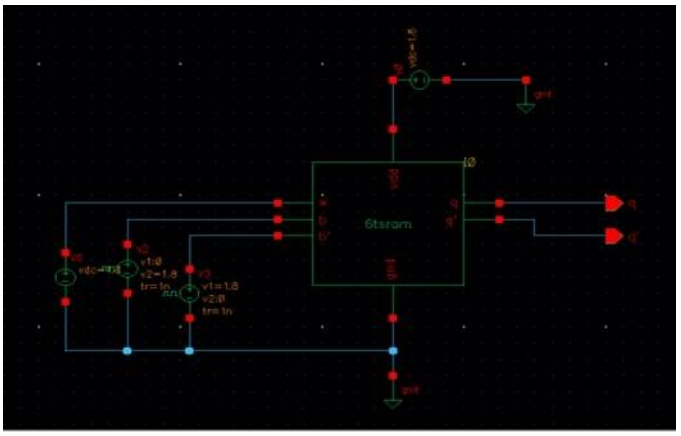

Fig 3 : Test bench of 6T SRAM

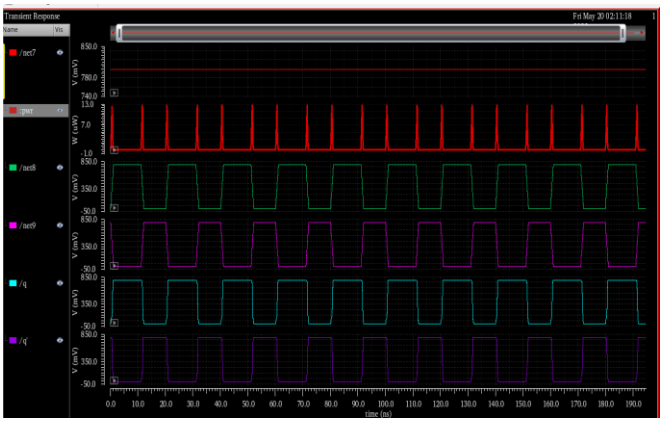

Fig 4: Power Analysis Waveform of 6T SRAM

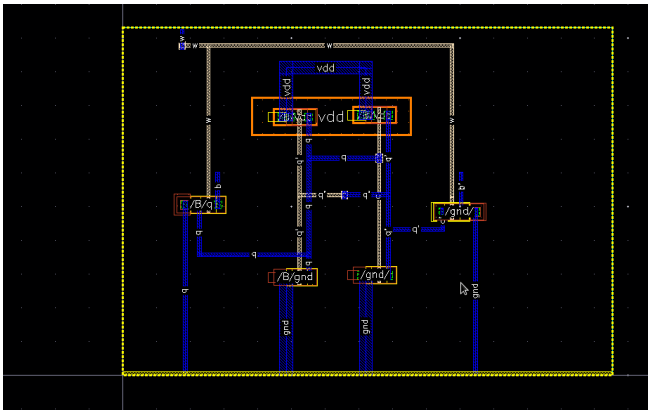

Fig 5: Layout of 6T SRAM

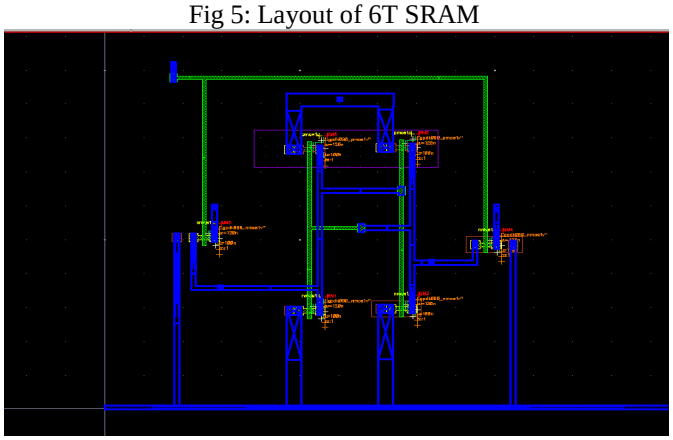

Fig 6: Av_extraction of 6T SRAM

8T SRAM using 90nm CMOS technology

The design of 8T SRAM in 90nm CMOS technology is doneusing Cadence tool. The schematic consist of word line (w1),input (b, b1) and output (q, qb).

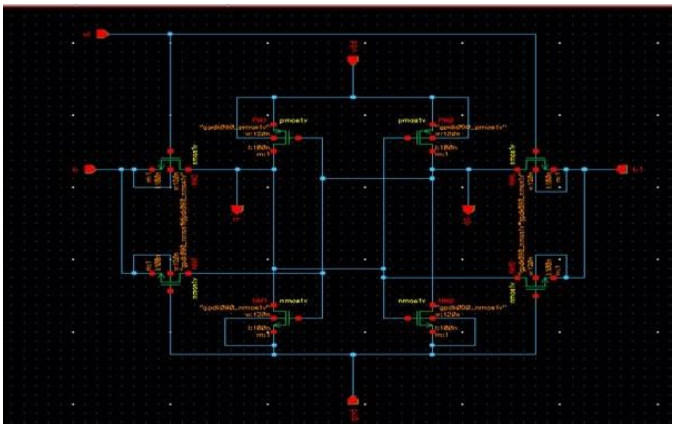

Fig 7: Schematic of 8T SRAM

In test bench, we have given the supply voltage (Vdc) as1.4v and input lower to higher voltages as 0v to 1.4v.

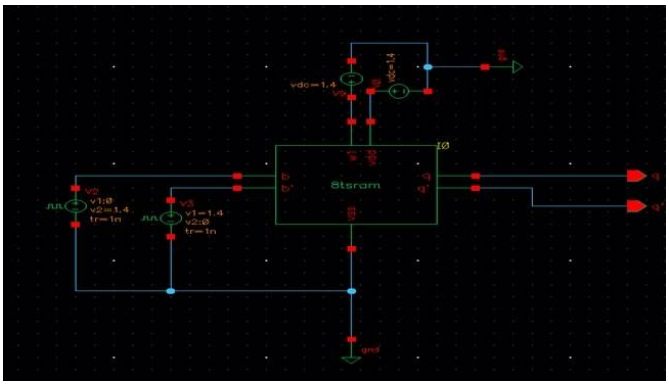

Fig 8: Testbench of 8T SRAM

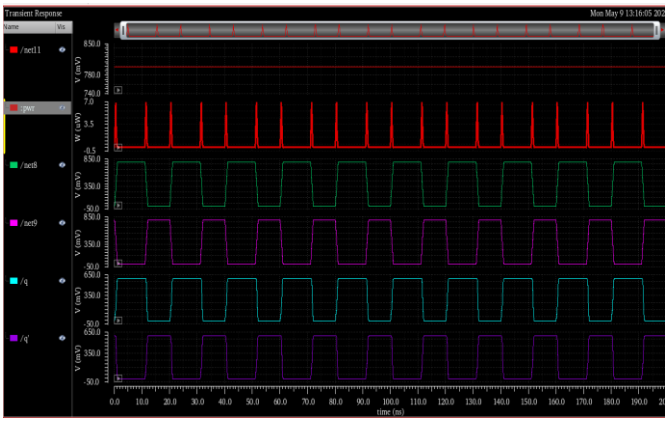

Fig 9: Power Analysis waveform of 8T SRAM

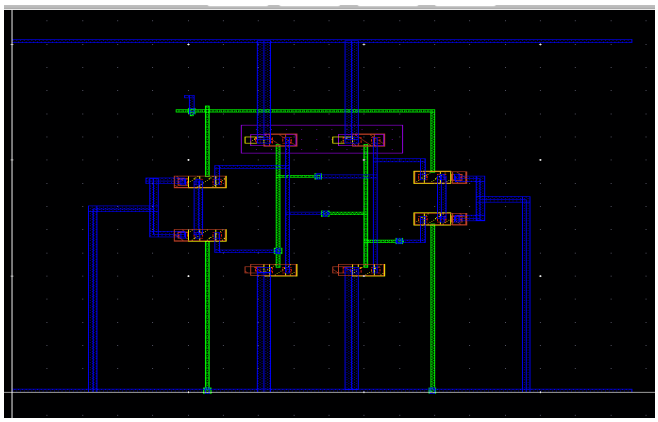

Fig 10 : Layout of 8T SRAM

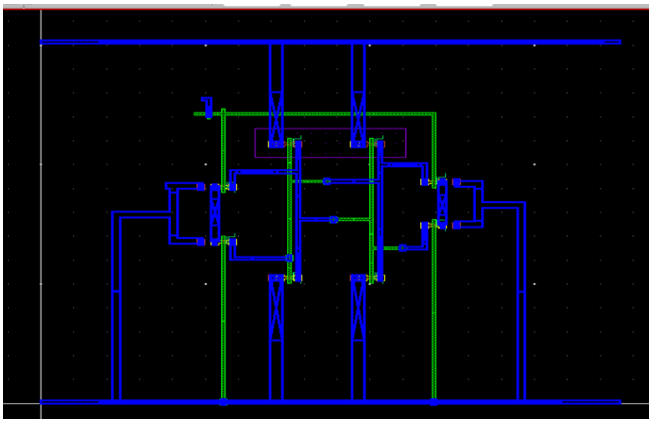

Fig 11: Av_extraction of 8T SRAM

III. Delay Analysis

Delay time depends on the critical voltage and W/L ratio of the transistors. The average delay of 6T SRAM cell and8T SRAM cell is observed.

ANALYSIS	6T SRAM	8T SRAM
Average delay (beforeback annotation)	9.262 E-4	9.857 E-4
Average Delay (AfterBack Annotation)	9.061 E-4	9.409 E-4

IV. Power Analysis

Power analysis is the rate of energy which is consumed from the source and converted into heat. Power dissipation can be minimized by different techniques, Low power supply voltage (VDD) is one of the most widely used technique to achieve low power dissipation. When low supply voltage is applied to SRAM it improves battery life.

ANALYSIS	6T SRAM	8T SRAM
Power Dissipation(Before back Annotation)	6.649 E-6	3.046 E-6
Power Dissipation(After Back Annotation)	6.716 E-6	3.179 E-6

V. Leakage Power Analysis

Leakage current is the current that flows in the circuit even when the transistor is turned off. Leakage power is the unwanted sub-threshold current in the transistor evenwhen the transistor in OFF mode.

Average delay = (rise time delay + fall time delay)/2Leakage Power = Leakage current * Vdd

ANALYSIS	6T SRAM	8T SRAM
Leakage Current	699.3 E-3	555.9 E-3
Leakage Power	1258.74mW	778.26mW

VI. CONCLUSIONS

Embedded memories implemented with 6T SRAM cell occupy a large portion of cryptographic systems and may hold secret data, these require special design steps to provide resiliency to leakage power attacks. In this project we have implemented a 6T and 8T SRAM cell using Cadence software tool. It is observed that 6T SRAM has lesser delay than 8T SRAM cell. The Power dissipation and leakage power is more in 6T SRAM when compared to 8T SRAM. Since 6T SRAM cell has more leakage power it is easier for the attacker to extract the data through side channel leakage information. Designed 8T SRAM cell provides less leakage power thereby reduces the risk of attacks and helps us to maintain our secrecy.

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