International Journal of Research in Engineering and Science (IJRES)
ISSN (Online): 2320-9364, ISSN (Print): 2320-9356
www.ijres.org Volume 10 Issue 7 ǁ July 2022 ǁ PP. 136-140

Analysis and Implementation of Cascaded Multilevel Inverter Topologies

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Abstract: *People working in the control and distribution of energy have taken notice of the benefits of utilising multilayer inverters in high-power applications with minimal harmonics. Multilevel inverters enable the use of renewable energy sources in addition to achieving high power ratings. The multilevel inverter's primary purpose is to combine many levels of DC voltages into the necessary high voltage. Sources of these DC voltage levels can include fuel cells, batteries, and other DC voltage sources. Using this technique, switching angle, phase delay, and pulse width may be determined for excellent waveform and reduced THD. The MATLAB/SIMULINK platform is used to implement this inverters model.*
Keywords: *Multilevel, Economic, THD, Simulink model.*

Date of Submission: 24-06-2022 Date of acceptance: 05-07-2022

I. INTRODUCTION

The multilevel inverter has generated a lot of attention in the high-power business lately. They offer the most recent collection of elements that may be used to simplify reactive power adjustment. Without the use of transformers or series-connected synchronized switching devices, multilevel voltage source inverters' distinctive configuration enables them to reach high voltages with minimal harmonics. The Diode clamped, Flying capacitor, and Cascaded H-bridge inverter is the three main different inverter structures which are used in industrial applications with separate dc sources [1-5]. A diode-clamped multilevel (m-level) inverter (DCMLI) consists of (m-1) capacitors on the dc bus and produces m levels in the phase voltage. Some of the features are as follows:

- Blocking diodes with a high voltage rating.
- Unbalanced capacitor voltage.
- Unequal switching device rating.

However, the voltage level for the flying capacitor converter is identical to that of the diode-clamped converter. In flying capacitors, the order is numbered differently from that of the diode-clamped inverter [6-8]. Additionally, this has the following qualities:

- Balancing capacitor voltages.
- A Large number of capacitors.

A cascaded-multilevel inverter is made up of many H-bridge inverter components. With the use of multiple different dc sources, such as fuel cells, batteries, or solar cells, this multilayer inverter can provide the desired [9-11]. voltage. It has some characteristics:

- The cascaded inverters require distinct dc sources for power conversions from ac to dc or vice versa. It is appropriate for a range of renewable energy sources, such as solar, fuel cells, and biomass.
- It is not feasible to connect two converters back-to-back with DC sources because a short circuit might be created.

Cascaded H-bridge inverters solve the capacitor voltage balancing issue that plagues flying capacitors and diode-clamped inverters. Asymmetric and symmetric cascaded multilevel inverters are the two classes into which the cascaded topologies are divided. Due to the varying amplitude of its dc voltage source, the asymmetric CMLI produces a greater number of output levels than the symmetric CMLI [12]. The cascaded H-bridge multilevel inverter uses asymmetric voltage methods to raise the no output voltage levels. Voltage levels can be raised by using cascaded bridge MLI. Cascaded multilevel inverters' primary advantages are their uniform design and packaging. This results in a quicker and less expensive production process [14]. This has the drawback of requiring a separate dc supply for each H-bridge and having a large number of power switches. Sine Property methods may be used to precisely control the majority of cascaded inverter characteristics.

II. 3-LEVEL CASCADED H BRIDGE INVERTER

Each H-bridge in a basic H-bridge inverter includes four semiconductor switches, and the four cells [15] can output voltage with either positive or negative polarity or zero volt due to the switching behaviour of the switches as shown in Fig. 1.

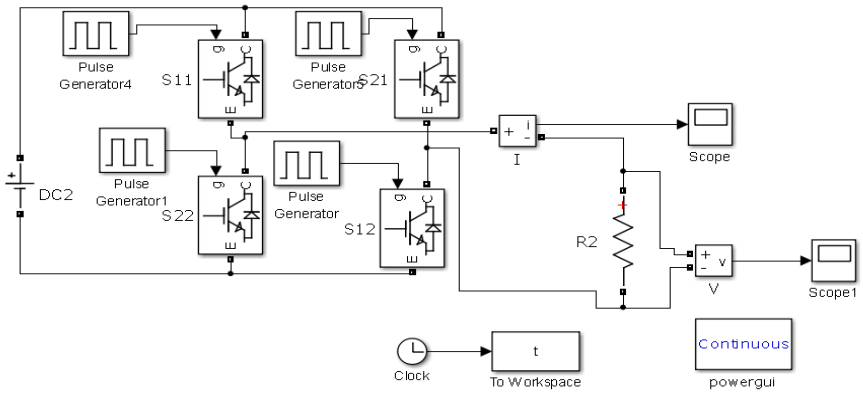

Fig.1 MATLAB circuit for 3-Level Cascaded H-Bridge Multilevel Inverter

Three levels are the lowest possible number of voltage levels for a multilevel inverter using a cascaded arrangement. Full-bridge inverters, also known as H-bridge cells, are used to illustrate how switches change ON and OFF by the switching voltages of a single H-bridge since they are necessary to obtain a waveform with three levels as shown in

Table 1: Output Voltage Values for H-bridge

Switching Voltage	**S11**	**S12**	**S21**	**S22**
0	1	1	0	0
Vdc	1	0	0	1
0	0	0	1	1
0	0	0	1	1
-Vdc	0	1	1	0
0	1	1	0	0

Table1. Three output switch levels, +V, -V, and zero, can be taken into consideration for voltages across the load according to a single H-bridge, which performs four switching operations.

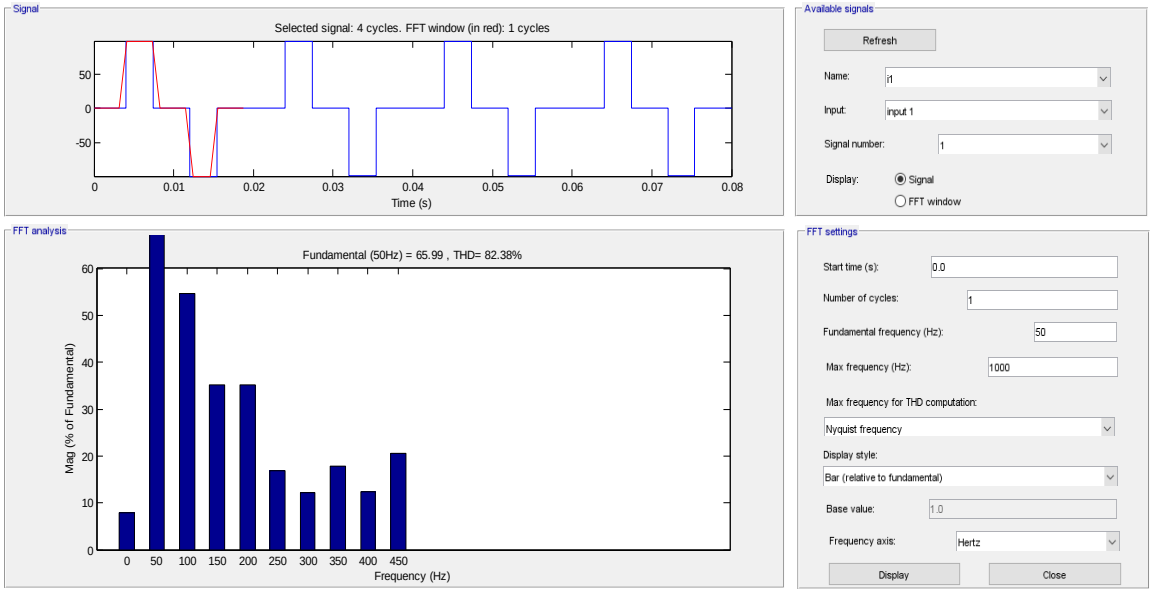

Fig.2 3 level inverter Simulated waveform of output voltage and THD

III. 1. 5-LEVEL CASCADED H BRIDGE INVERTER

The performance analysis has been analyzed of 5 level inverter is shown in Fig.3. This inverter consists of the series connection of two H –bridges fed with two voltage sources. The output voltages of the inverter are the sum of all voltages that appear at each cell output. The output voltage is given by $V=V_1 +V_2$, Where V_1 appear across the first cell and V2 appears across the second cell. For a five-level inverter the output voltage ie. 2V, V, 0, -V, -2V.

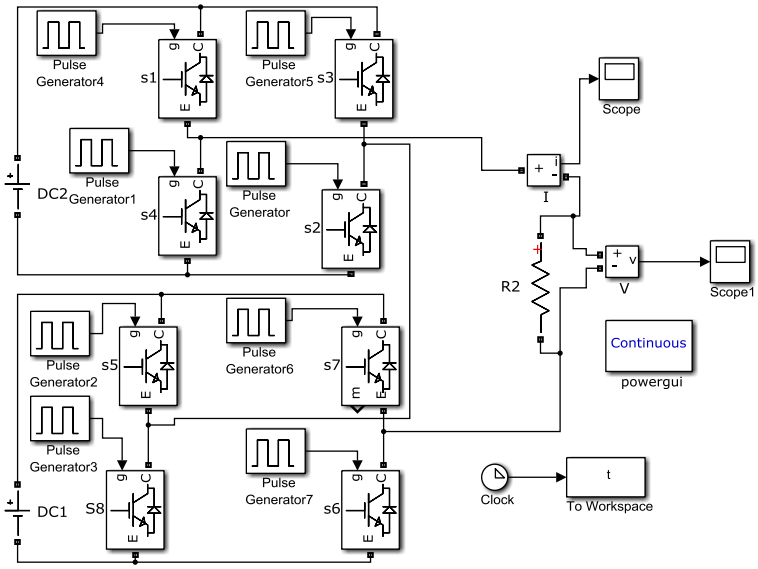

Fig.3 MATLAB circuit for 5-Level Cascaded H-Bridge Multilevel Inverter

III. 2. WORKING OPERATION OF FIVE-LEVEL INVERTER

Mode1: In mode1 operation switches S_1, S_3, S_5, and S_7 are on. The output voltage obtained across the load is zero.

Mode 2: In mode2 operation switches S_1, S_3, S_5, and S_8 are on. The output voltage obtained across the load is $+V_{dc2}$.

Mode 3: In mode3 operation switches S_1, S_4, S_5, and S_8 are on. The output voltage obtained across the load is $V_{dc1} +V_{dc2}$.

Mode 4: In mode 4 operation switches S_2, S_4, S_6, and S_7 are on. The output voltage obtained across the load is $-V_{dc2}$.

Mode 5: In mode 5 operation switches S_2, S_4, S_6, and S_8 are on. The output voltage obtained across the load is 0.
Mode 6: In mode 6 operation switches S_2, S_3, S_6, and S_7 are on. The output voltage obtained across the load is $-V_{dc1} - V_{dc2}$.

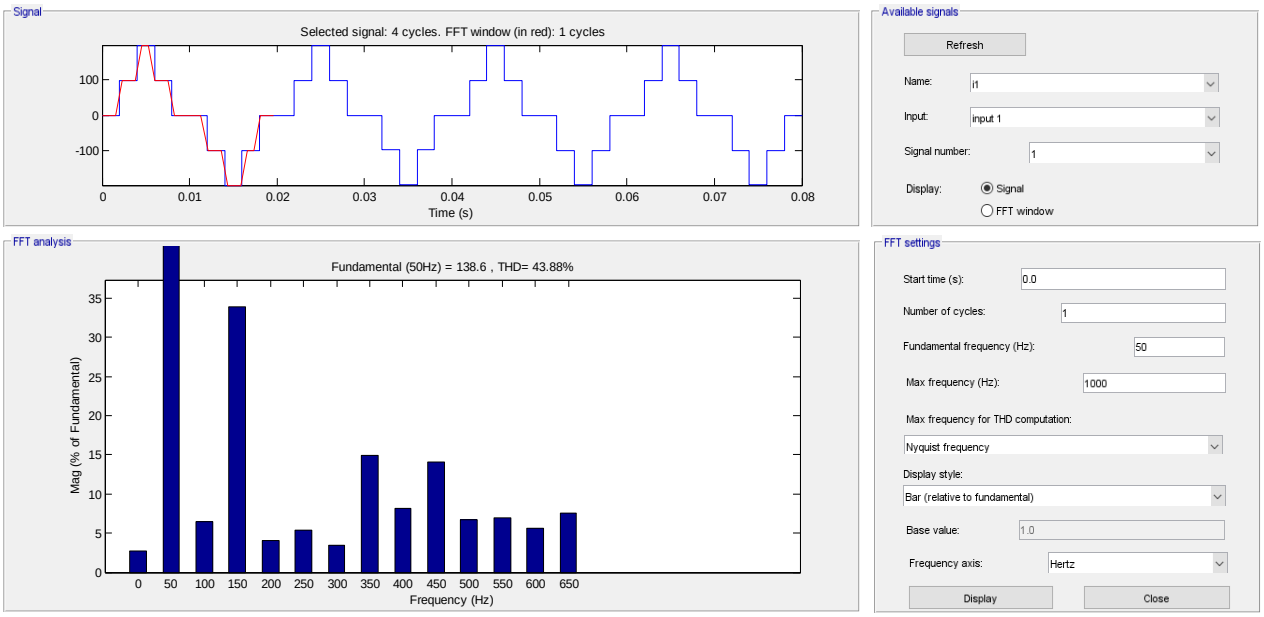

Fig.4 5-level inverter Simulated waveform of output voltage and THD

Table. 2 THD analysis of 3 & 5 level inverter

S. No	Types of multilevel Inverter	Total Harmonics Distortion with R Load
1	3 level	82.3%
2	5level	43.68 %

IV. CONCLUSION

As the multi-level inverter topologies are studied the possibility of producing a higher number of levels with the same switches as in conventional topology is made. The performance analysis has been made by the simulation of 3 levels and 5 levels inverters using MATLAB. As result, it clearly shows as the level of inverter increases the THD will decrease and the output waveform goes the acquire more and more sine waves. So the quality of output voltage and current will improve, and losses will be minimized as we approach a higher level of the multilevel inverter.

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