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Reliable and Efficient Design of Network-On-Chip

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ABSTRACT
This paper present a method for designing fault tolerant reliable and efficient NoC. It involves new error detection and correction method to protect the NoC from transient and permanent errors, there by accurately localize the position of faulty blocks in the NoC routers. Routing algorithm is the key factor in NoC architecture. The proposed NoC is based on modified XY routing algorithm combined with a scheduler and an elastic buffer. It's a very fast way to transferring data packet through a specific path between source and destination nodes in the network. Collision can be prevented by using a scheduler and queuing procedure is providedby using an elastic buffer. This is a promising technique with reliable and high error tolerance.
Keywords – *Network on Chip (NoC), Routing algorithm*

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I. NTRODUCTION

Network on chip (NoC) is an important paradigm for implementing communication among various cores in SoC and NoC medium features a high level of modularity, flexibility and throughput [1]. In NoC architecture, the chip is divided into set of interconnected blocks where each node can be a general purpose processor, which iscommonly known as processing element (PE) [2]. The NoC relies on data packet exchange. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm [1], [2]. A typical NoC consist of switches, links and Network Interfaces (NIs). A NI connects a core to the network and co-ordinates the transmission and reception of packets from/to the core. A packet is usually segmented into several flow control units (flits). The switches and links are used to connect the various cores and NIs together [1]. To achieve a reconfigurable NoC, an efficient dynamic routing algorithm is required for the data packets. The goal is to preserve flexibility and reliability while providing high NoC performance in terms of throughput [1], [3], [6].Fig.1 shows the dynamic reliable NoC and its communication between several IP and bypass determined by the dynamic routing algorithm [1].

The proposed NoC is a mesh structure of routers able to detect routingerrors for adaptive routing based on the XY algorithm [1], [3], [7]. The approach includes data packet error detection and correction. The originality of the proposed architecture is its ability to localize accurately error sources, allowing the throughput and network load of the NoC to be maintained [4]. The routing algorithm is based on the adaptive turn model routingscheme and modified XY algorithm with a scheduler. The adaptive algorithm is live lock and deadlock-free and allows data packets to pass around faulty regions [1].

The remainder of this paper organized as follows. Section II describes the existing techniques and disadvantages. Section III will explain the proposed technique. Section IV consists of results and discussion of the project, finding and analysis thought the thesis and project development. Finally, conclusions and reserves suggestion forpossible researches.

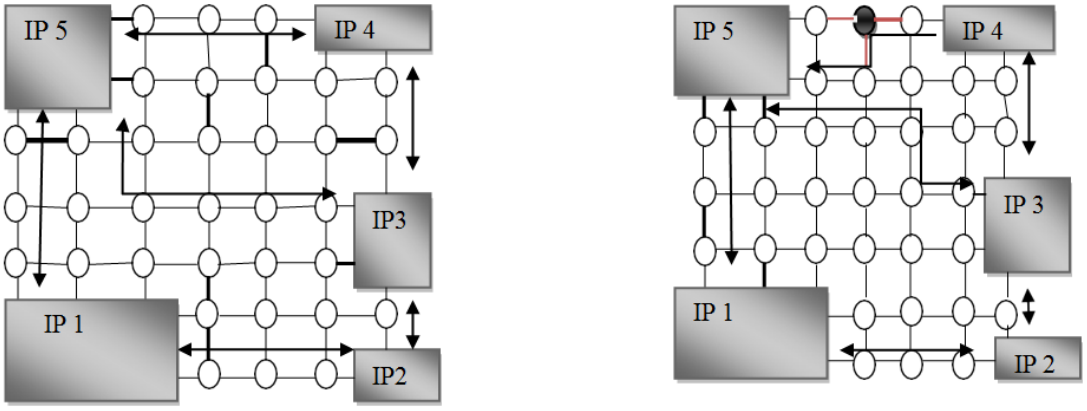

Fig.1.Illustration of a dynamic NoC. (a) Normal operation. (b) Online detection of a faulty router.

II. EXISTING TECHNIQUES

The reliable switch incorporates an online routing fault detection mechanism. This approach can operate with adaptive algorithm based on normal XY routing algorithm [1], [3], [5], [7]. This algorithm routes packets first in horizontal direction to the correct column and then in vertical direction to the receiver. In this algorithm router addresses are the XY coordinates. XY routing algorithm avoids deadlock and live lock situations. A routing table is associated with this algorithm, it contain the output port to use for each destination in the network [6]. These tables are updated by initialization algorithm. Drawback of this solution is the requirement to invoke the algorithm at non specified time in order to update the table.

A.ROUTING ALGORITHM

Routing algorithm is a key factor which affects the efficiency of the communication of NoC [3]. The routing algorithm, which defines the path between source and destination. The choice of routing algorithm depends on trade off between several potentially conflicting metrics like minimizing logic. There are two types of routing, which is source and distributed routing. In source routing, whole path is decided at the source router, while in distributed routing each router receives a packet and decides the direction and send the data packet. The path is uniquely defined by the source and destination, in between any faulty or unavailable region occurs it will bypass. The main difficulty in routing error detection is to distinguish a bypass of an unavailable component in the NoC from a real routing error [1], [3], [8]. Fig.2.shows the routing error detection problem.

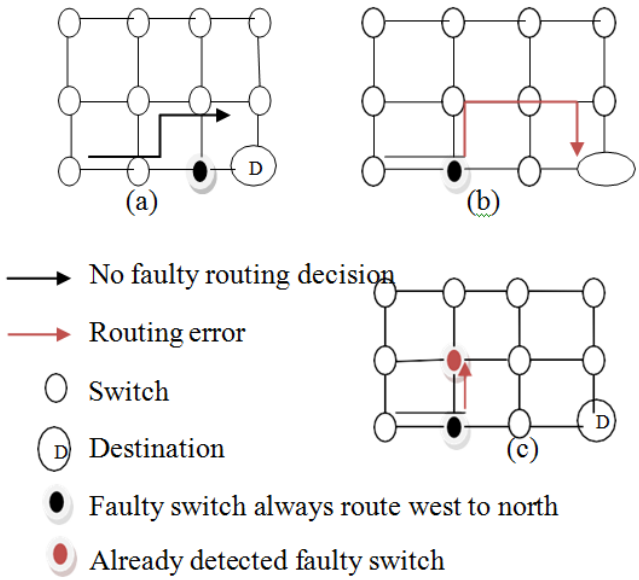

Fig.2. illustration of routing error detection problem (a) dynamic bypass (b) routing error (c) to avoid loss of data packets.

An important problem in existing NoC design is communication and task scheduling. Bypassing and scheduling problems can be considered jointly. However, finding the optimum solutionremains an open problem due to its complexity [3], [7]. Existing XY routing algorithm causes the biggest load in the middle of the network which does not extend the traffic regularly over the network.Thus there is a need for algorithms which equalize the traffic load over the whole network and are yet simple and efficient [6].

III. PROPOSED TECHNIQUE

The proposed method uses a modified XY routing algorithm combined with ascheduler and a buffer to avoid the traffic congestion. The method uses a 48 bit data packet. Fig.3 shows the packet format. First 3 bits indicates don't care, then request bit,is initially set to 0 and is used by the scheduler, followed by 32 bit data. The last6 bits are the destination address and source address. For routing the scheduler will setthe request bit for these nodes to 1 and will further schedule these nodes to send the data. All packet having request bit is undergoes for the modified XY routing algorithm depends upon the priority given by the arbiter. Packets are store in FIFO unstill it get grand signal from arbiter. Once get grand signal actual XY routing takes place.

XXX	1	DATA	DESTINATION ADDRESS	SOURCE ADDRESS

Fig.3. Packet format

A.DYNAMIC FAULT HANDLING

NoC operating system monitoring utilization of routers and switches, power consumption and error statistics, diagnostic and fault recovery. In the case of modular distributed system, each programmable component will be provided with system software to supportits own operation. Communication ismanaged with the on chip network and interacts with neighboring componentssystem software. If a resource becomes faulty, NoC operating system detects a faulty resource and defines a new region to isolate the faulty resource [5]. Finally, NoC reconfigures the network layer protocol.

Recovery mechanism associated with a switch, which route packets based on the entire network statistics and other members of the society. This algorithm could operate as a deterministic or adaptive routing depends on neighboring switches load condition. When congestion becomes high, agent tries to route packet through less congested path. This can be achieved by using 2 bit quantized load value, so each agent has 4 quantized value that are sent to 4neighbors, that is north,south,east,west. As showed in Table 1. Configuration packetsare generated according to the information received from all neighbors.

Table 1

00	Port is ready and ready to receive
01	Threshold 0(50% of buffer is full)
10	Threshold 1(75% of buffer is full)
11	Port is quite busy and cannot receive

B.DESIGN OUTLINE

The routing algorithm comprises of twomain functions. One relates to gathering ofresources and the other is, making a decisionbased on the information collected. Fig. 4 shows the simplified block diagram of tworouters with buffer queue. From theperspective of router 1, the link connects thenext-hop switch allocator to a local FIFO; which encapsulates route calculation logic. The buffer count works as follows, from theperspective of router 1, if the local writesignal is logic high, the count incrementsand, if the read enable signal from router 2goes high, the count decrements [8].

Router 1 records the status of its east output port; the west FIFO of router 2. This functionality is repeated for all cardinal directions. The main routing algorithm utilizes the buffer count functionality andwill contain conditional statements to check for a productive path less than a threshold. Ifunavailable, it checks all unproductive caseswith unique boundary conditions to find the smallest queue. Packets are routed productively regardless of comparison to the threshold if no single smallest path exists. Boundary conditions have to be considered because, depending on the position of the router, the possible next hop paths to compare and route

along are different[8].

Flow control is needed in networks to support full throughput operations. Specifically, it is needed to ensure that enough buffering is available at each switch to store the incoming data and the available buffers are utilized efficiently. Queuing buffers are either located at the input (input- queued switches) or at the output (output queued switches). In some switches, the buffers can be located at both the inputs and the outputs to improve the performance of the NoC.

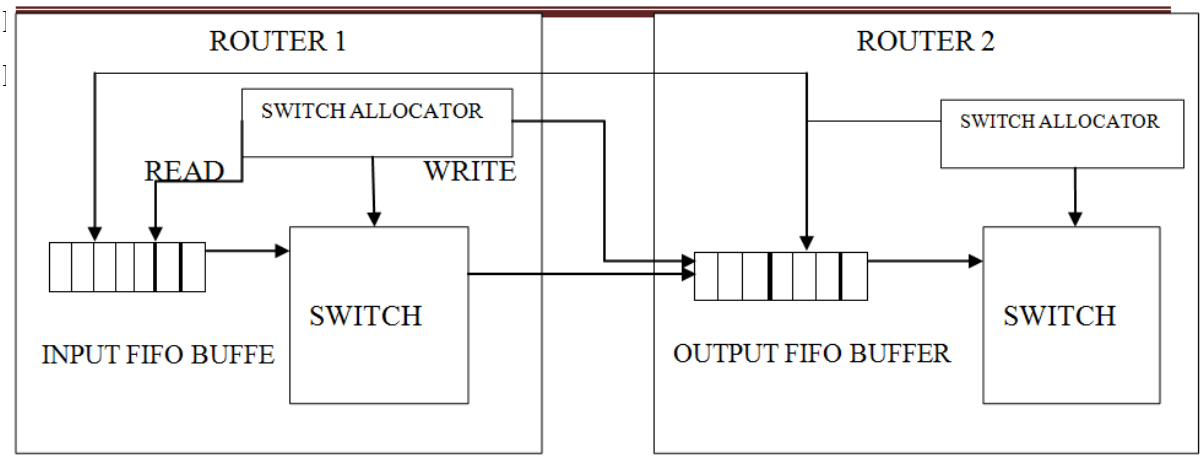

Fig.4. simplified block diagram of two routers with buffer queue

IV. RESULTS

Reliable and efficient NoC was designed and implemented in this project. The system was first modeled in MODELSIM and the algorithm was verified. Later based on this algorithm the high level and low level architecture was designed. Xilinx 14.2 ISE Synthesis Technology (XST) as our synthesis environment, the RTL and Technology viewers allow viewing aschematic representation of synthesized net list. The designed architecture was RTL coded in Xilinx ISE 14.4 using verilog hardware description language and synthesized. The synthesized design was simulated in ISim simulator. Finally the design was ported to XC3S250E Sparten-3E Xilinx FPGA Evaluation Development Board and the results were analyzed. Once the functional verification are done, the RTL model was taken to the synthesis processusing the Xilinx ISE tool. In synthesis process, the RTL model will be converted tothe gate level net list mapped to a specific technology library. Table 2 shows the device utilization summary. The deviceutilization summary is shown as design summary in which it gives the details of number of devices used from the available devices and also represented in percentage.

FLOWCHART

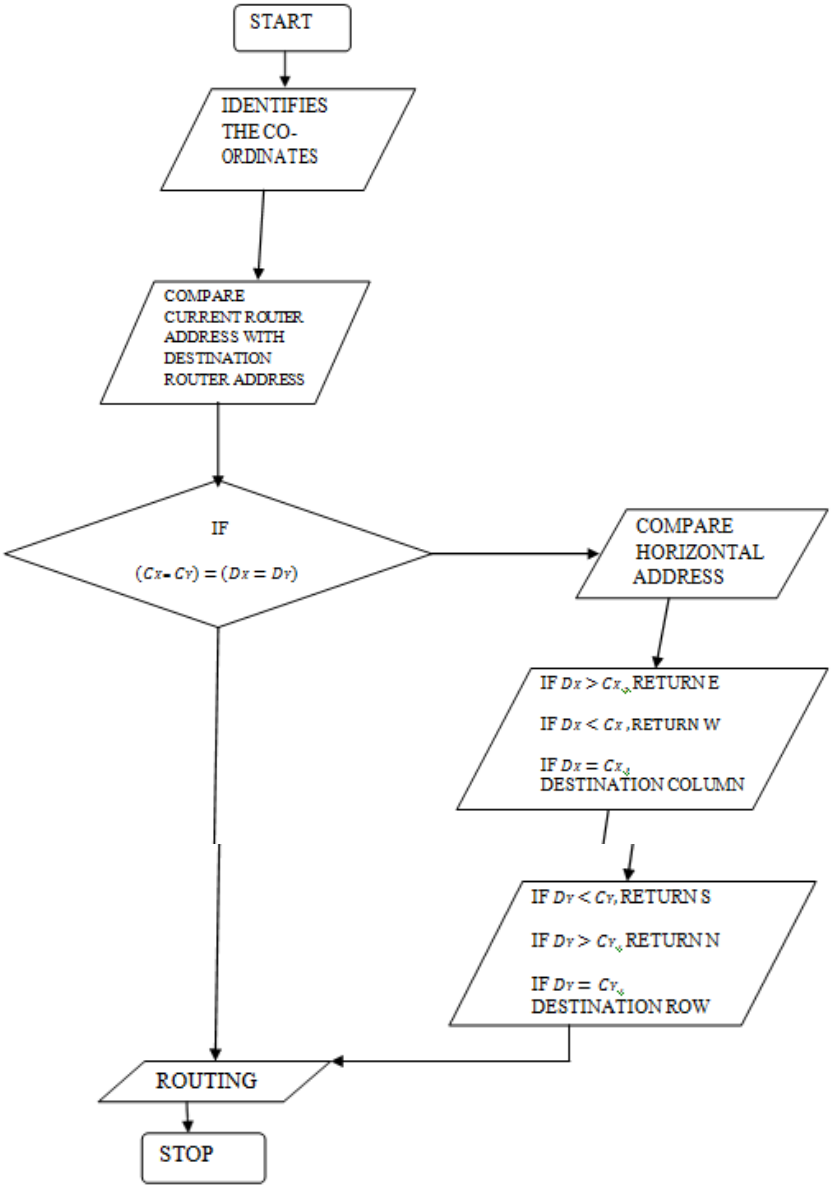

Table 2: Device utilization summary

Logic Utilization	Used	Available	Utilization
Number of Slices	120	2448	4%
Number of 4 inputLUTs	250	4896	5%
Number ofbonded IOBs	22	108	20%
Number of GCLKs	1	24	4%

Timing summary

Minimum period: 5.632ns Maximum frequency: 177.55MHz
Minimum input arrival time before clock:13.606ns
Maximum output required time after clock:17.478ns
Maximum combinational path delay:18.143ns

V. CONCLUSION

The ideas presented in this paper make the NoC architecture resilient to permanent and transient or intermittent errors by using a modified XY algorithm and a control circuitry is used for simply controlling or queuing the bit line or data packets. This is the fast and efficient way to transferring data packet through a specific path between two nodes in the network and the scheduler further helps to avoid collision. The use of non intersecting paths achieves the fault tolerant routing. the proposed routing error detection mechanisms allow the accurate localization of permanent faulty routing blocks in the network. They are suitable for adaptive routing algorithms based on XY, where the main difficulty is to distinguish the bypass of an unavailable component in the NoC. Validation simulations of proposed routing error detection showed a routing error localization close to 96% for routing errors on an modified XY algorithm in a4×4 NoC.

In future the entire scheme presented to improve the reliability of the NoC architecture has power overhead associated with them. This increases the power dissipation, which can reduce the mean time to failure. Most error resilient schemes today focus primarily on making router, links and fault tolerant, these should be some focus onmaking memories more reliable.

REFERENCES

[1]. Cedric Killian, Camel Tanougast,Fabrice Monteiro and Abbas Dandache,"Smart Reliable Network-on-Chip" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.16, no.10, pp.1400-1408, Oct 2013.
[2]. A. Ejlali, B. Al-Hashimi, P. Rosinger, S. Miremadi and L. Benini,"performability/energy tradeoff in error- control schemes for on-chip networks",IEEE Trans. Very Large Scale Integr.(VLSI)Syst., vol.18, no.1, pp.1-14, Jan 2010.
[3]. K.Sekar, K.Lahiri, A.Raghunathan and S.Dey, "Dynamically configurable bus topologies for high performance on-chip communication" IEEE Trans. Very Large Scale Integration (VLSI) Systems, vol.16,no.10, pp. 1413-1426, Oct 2008.
[4]. S. Murali,T. Theocharides, N. Vijaykrishnan, M. J. Irwin, L. benini, G. De Micheli, "Analysis of Error Recovery Schemes for Network-on-Chip", IEEE Design and Test of Computers, vol.22(5),pp.434-442, Sep-Oct 2005.
[5]. F.Worm, P. Ienne, P. Thiran, and G.De Micheli, "A Robust Self-calibrating Transmission Schemes for On-Chip Networks," IEEE Transactions on VLSI, vol.13 (1), pp.126-139, Jan 2005.
[6]. D. Bertozzi, A. Jalabert, S. Murali, R. Tamahankar, S. Stergiou, L. Benini,G. De Micheli, "NoC Synthesis Flow for Customized Domain Specefic Multiprocessor Systems-on-Chip", IEEE Transactions on Parallel and Distributed Systems, pp.113-129, vol.16, no.2, Feb.2005.
[7]. J. Wu, "A fault-tolerant and deadlock- free routing protocol in 2d meshes based on odd-even turn model", IEEE Trans. Comput. Vol.52, no.9, pp.1154-11169, Sep.2003.
[8]. L.P. Carloni, K.L. McMillan, A.L.Sangiovanni Vincentelli "Theory of LatencyInsensitive Design," IEEE Trans. on CAD ofICs and Systems, vol.20, no.9, pp.1059- 1076, Sep 2001.