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Effective control of short channel effect in Multimaterial cylindrical all around MOSFET

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Abstract
In this article, a cylindrical MOSFET with Dual Material and Double Gate is designed, which has two gates with two different Gate materials. The proposed structure is named as Dual Material Double Gate-Cylindrical Gate All Around (DMDG-CGAA) MOSFET structure. In this structure tubular channel is controlled by the inner gate and the outer gate. The inner gate enhances charge control in the channel region because the inner gate is surrounded by the oxide layer. And the outer gate is similar to the GAA devices. Both the inner gate and the outer gate have two different materials with different work functions. These two materials are from source to drain are: Aurum Au (ϕm_1 = 4.8eV), Titanium Ti (ϕm_2 = 4.4eV). The ratio of the channel length L_1:L_2 is 1:1. The channel region of the device is lightly doped with the acceptor concentration ($N_A = 1\times10^{18}$ cm-3) and the source and drain regions are highly doped with the donor concentration (N_D = 2× 1020 cm-3). 3D ATLAS tool from SILVACO is used for all the device simulation. Threshold voltage, trans conductance and DIBL calculations is done and compared with SG-CGAA MOSFET, DG-CGAA MOSFET, DMDG-CGAA MOSFET. By comparing all these structures, it can be concluded that the immunity of SCE is enhanced in the proposed structure.

Keywords: *SCEs, DMDG CGAA MOSET, DIBL, Threshold voltage*.

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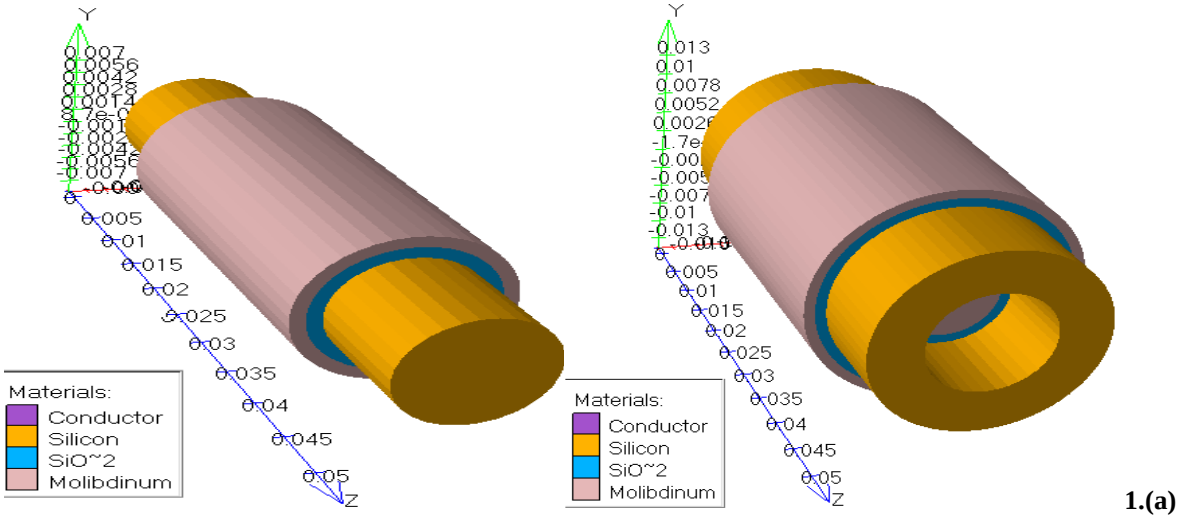
I. INTRODUCTION

MOSFET has been the main interest of research in semiconductor industries because of its low power dissipation, greater package density, and superior performance. But the thrust of decreasing dimensions of chips leads to various undesirable effects which are known as short channel effect. DIBL, punch through, channel width modulation, velocity saturation is some of these affects which degrade the device performance [1-4].

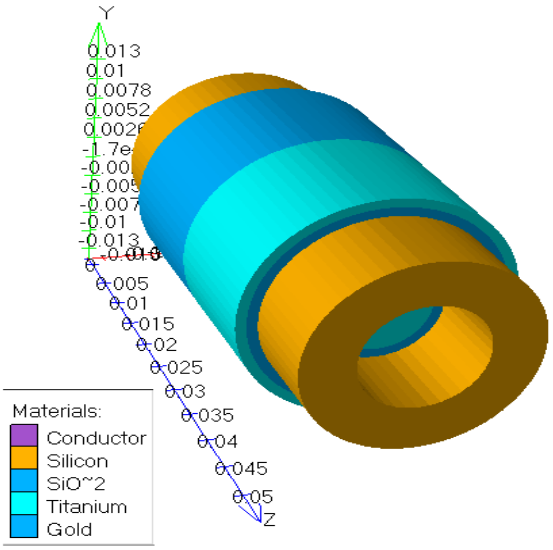
A promising solution of these issues are addressed by some alternative non-conventional devices. Multiple gate devices are one of the solutions among them for nanoscale technology. Multiple gate devices are a strong candidate for scaled devices in the nanometer regime because of its excellent immunity to the short channel effect (SCE), decreases the leakage current, device driving controllability increases and also the output resistance of the device becomes high. Threshold voltage roll-off and Drain Induced Barrier Lowering(DIBL) are two main short channel effects, due to these effects the off current enhances in the off state of the transistor, which leads to a decrease in the on-off current ratio. In the multiple gate devices, the electrostatic control of the channel by gate electrode increases by which the SCEs are reduces and the mobility problem decreases by using the lightly doped channel region. SCE can be controlled in the multigate 3D transistors by controlling the effective channel length [5-8]. Many multigate devices like a double gate, triple gate and Gate All around (GAA) structures are used to further reduce the SCE in the nanometer regime. Among all these proposed structures the GAA devices have better gate control because in the GAA structure the gate is wrapped from its all sides [9-10]. For further downscaling the Cylindrical Gate All Around (CGAA) MOSFET is one of the most promising devices. In this design, the channel is completely surrounded by the gate so gate control increases which reduce the SCEs. When the material engineering is combined with the gate engineering the performance of the CGAA increases. In this article a cylindrical MOSFET structure is proposed, in this cylindrical MOSFET, two gates are wrapped around the channel region with two materials. This design shows better electrical characteristics like drain current, threshold voltage, trans conductance as drain current, threshold voltage, trans conductance as compared to planar MOSFET and other CGAA MOSFET.

II. DEVICE STRUCTURE

Fig.1. (a), (b), (c) represents the simulated structure of different type of cylindrical MOSFETS i.e. cylindrical Gate All Around MOSFET (CGAA), Double Gate-Cylindrical Gate All Around (DG-CGAA) and Dual Material Double Gate-Cylindrical Gate All Around (DMDG-CGAA). These MOSFETs structures are also having source, drain, channel, oxide and gate region similar to conventional MOSFET.



1. (b) **1.(a)**



1(c)

Figure 1: (a) Simulated structure of CGAA MOSFET (b) Simulated structure of DG-CGAA MOSFET (c) Simulated structure of DMDG-CGAA MOSFET

In CGAA structures a single gate of Molybdenum which is of cylindrical shape is covering the tubular channel from all around. Whereas in DG-CGAA two cylindrical gates are used. The internal gate acts as a backbone to the whole structure on which inner gate oxide, channel, outer gate oxide, outer gate are wrapped respectively. This device is having symmetrical structure and inner and outer gate terminals are supplied the same gate voltage. In addition to these features, in DMDG structure two dissimilar material is used for both inner and outer gate. These two materials from source to drain is: Aurum Au (ϕ_{m1} = 4.8eV), Titanium Ti (ϕ_{m2} = 4.4eV). The ratio of the channel length L_1:L_2 is1:1. The channel region of the device is lightly doped with the acceptor concentration ($N_A = 10^{18}cm^{-3}$) and the source and drain regions are highly doped with the donor concentration ($N_D = 2\times 10^{20}$ cm^{-3}). The SiO_2 is used as the gate oxide.

Table I indicates the design parameters for the DMDG-CGAA MOSFET. Si thickness is taken as 5nm for all the CGAA design structures. The gate oxide thickness (t_{ox}) is 1nm. The Sio_2 is used as the gate oxide with the dielectric constant equal to 3.9.

TABLE I. List of design parameters of TMDG -CGAA MOSFET

Parameters	Symbols	Values
Combined Channel Length	L_G	30 nm
Metal Channel Length M1 &M2	L_{G1}, L_{G2}	15 nm
Doping Concentration of channel	N_A	1×10^{18} cm^{-3}
Doping Concentration of Source and Drain	N_D	2×10^{20} cm^{-3}
Molybdenum work function (AU)	ϕ_{m1}	4. 8 eV
Titanium Work function (Ti)	ϕ_{m2}	4. 4 eV
Oxides thickness	t_{ox}	1 nm
Channel thickness	tsi	5 nm
Core Radius	R	5 nm
Length of Source/Drain	L_S/L_D	10 nm

III. RESULTS AND DISCUSSIONS

Fig.2.shows the voltage current characteristics where drain current is plotted w.r.t. gate voltage for SG CGAA MOSFET, DG CGAA MOSFET and DMDG CGAA MOSFET. Characteristics are obtained when the gate to source voltage is varied between the 0V to 1V and drain to source voltage is kept constant V_{DS} = 1V. It is observed from the characteristics that value of drain current is maximum in case of DMDG CGAA MOSFET because In the double gate structure the value of the drain current increases due to both inner gate and outer gate [11-17]. The channel region is controlled by both the gates and also two different gate material are used so the drain current enhances.

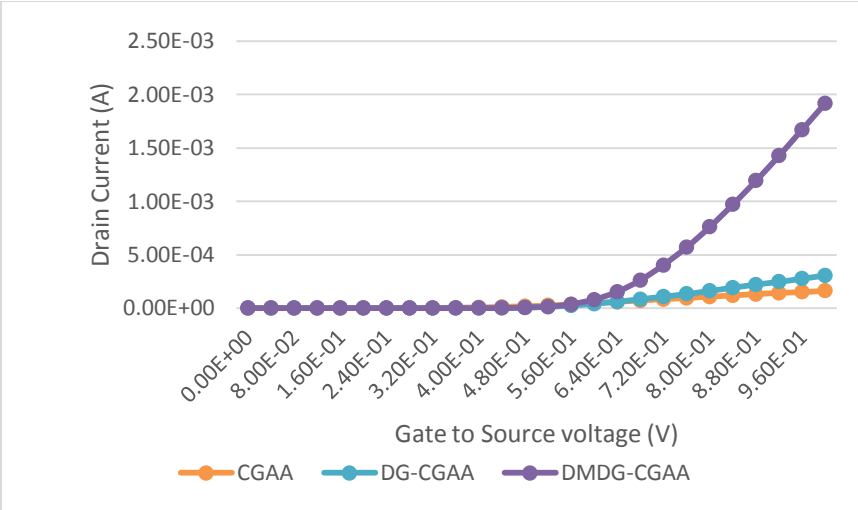


Figure 2: Transfer characteristics of CGAA, DG CGAA MOSFET, and DMDG CGAA MOSFET at 30nm channel length

To calculate Threshold Voltage, DIBL, Transconductance logarithmic version of the above graph followed by constant current method can be used [18-19] or threshold voltage can be extracted by simulation also. Channel length for all three structures is kept 30nm.

DIBL is known as the V_{th} variation at V_{DS}= 0.1v and V_{DS}= 1.0 to the V_{DS} variation V_{DS}= 1v and V_{DS}= 0.1v.

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} = \frac{(V_{th})_{V_{ds}=0.1v} - (V_{th})_{V_{ds}=1v}}{(V_{ds}=1v) - (V_{ds}=0.1v)}$$

The unit of the DIBL is mV/V.

Transconductance is determined by the ratio of change in I_D to the change in V_{GS}. g_m is the symbol and the unit is mA/V for the transconductance. In other words, higher transconductance gives higher amplifications. Transconductance can be calculated by the transfer characteristic of the device. The formula used for the transconductance is given as follows

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(I_D)_{V_{gs}=1v} - (I_D)_{V_{gs}=0.8v}}{(V_{gs}=1v) - (V_{ds}=0.8v)}$$

Table II, shows a comparison between the above mentioned three structure for the parameters like DIBL, threshold voltage, transconductance and maximum drain current. It is observed from the table that in case of DMDG CGAA MOSFET drain current is having maximum value, DIBL is having lowest value as 3.33mV/V, threshold voltage is 0.363V which indicates a better control on channel region, trans conductance is 4.90 mA/V which is highest among all three structures taken. So as it is clear from the results obtained that the DMDG CGAA MOSFET structures is having better immunity to SCE. Thus, by comparing and analyzing the results we can clearly say that DMDG CGAA MOSFET shows better characteristics in all aspects as compared to SG CGAA MOSFET and DG CGAA MOSFET devices.

TABLE II: Threshold voltage, drain current, DIBL and trans conductance of SG-CGAA MOSFET, DG CGAA MOSFET and DMDG-CGAA MOSFET

MOSFET structure	V_{th} (V)	Drain current (mA)	DIBL (mV/V)	Trans-conductance (mA/V)
SG-CGAA MOSFET	0.262	0.1628	5.55	0.3
DG-CGAA MOSFET	0.336	0.3052	4.45	0.715
DMDG-CGAA MOSFET	0.363	1.9	3.33	4.90

IV. CONCLUSION

In the proposed structure we aimed to get a MOSFET device which can have better control on SCE without compromising with maximum drain current and by obtained result in this work, it can be concluded that the proposed structure is achieving all these requirements. It has better DIBL (3.33 mv/V), superior transconductance (4.90 mA/V) better control over channel (Threshold voltage =0.36 V) with a higher (1.90 mA) maximum drain current than other conventional MOSFET at the same channel length of 30nm. This device combines the benefits of both the double gate structure and dual gate material. This device shows better gate electrostatic control over the channel region because of the Double gate and cylindrical structure.

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