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Design of DOCCCII in 16nm CMOS Technology

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Abstract
Advancement in VLSI technology has led to larger number of components on a single chip making it a reality to realise portable systems. Analog circuits are important in every VLSI system such as filters, current and voltage amplifiers, comparators, A/D and D/A converters, etc. Miniaturization in circuit design requires low-power low-voltage (LPLV) analog integrated circuits to be designed. Analog signal processing's inherent advantage of low power and high speed has led to extensive research in analog domain. Current domain processing having advantages of higher bandwidth, large dynamic range, greater linearity, simple circuitry seems to be the solution. Among the number of current mode topologies current conveyor is the most versatile building block. The second-generation Current controlled current conveyor (CCCII)has attained greater popularity in recent years due to electronic adjustability of X-terminal intrinsic resistance through bias current. Here we have designed dual output current controlled current conveyor (DOCCCII)in 16nm bulk CMOS technology using PTM (High Performance 16nm Metal Gate / High-K / Strained-Si parameter).

Keywords: *Analog circuits, Current mode, Current conveyor, Signal processing*

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I. INTRODUCTION

With scaling down of CMOS to comply with large scale integration and system on chip requirements together with increased demand for portable and battery-operated devices, low power low voltage (LP LV) devices are need of the hour. The current mode devices are more suited for (LP LV) operation than their voltage counterpart [1, 2]. Current mode circuits are more immune to noise, less sensitive to supply voltage and have low electrostatic discharge, low propagation delay, high slew rate etc. [2,4]. Among various current mode devices current conveyors (CC) is the most functional device by virtue of its versatile features such as simplicity in design, higher gain bandwidth product, linearity, high frequency operation, less chip area, low power dissipation [4-7] etc. In 1968 [1] the current conveyor (CC) was introduced and has since found recognition in both conceptual and practical implementation. Research published in last few years reveals that analog circuit designers are now considering the CC as a building block for designing multitude of applications like signal processing, amplification, instrumentation etc. [1,8,9]. A CC is a three terminal device having a low impedance input, a high impedance input simultaneously with a characteristic of virtual short and a high impedance output terminal [1,3]. Since its introduction many topologies of CC have been developed, but second generation current controlled current conveyor (CCCII) gathers larger attention from designers due to its high tunability [1,2,10]. CCCII has in built parasitic resistance, which is self-adjustable by bias current, due to this parasitic resistance the requirement of external resistance is reduced. Practical CC has various non-idealities and some of them prove their importance in different applications [11, 12]. Parasitic resistance of CCCII is one of its useful non idealities. Literature shows there are many tunable circuits i.e. current differencing transconductance amplifier (CDTA) [13], current follower transconductance amplifier (CFTA) [14,15], current controlled current conveyor transconductance amplifier (CCCCTA) [16-18], digitally programmable current conveyor (DPCCII) [19,20] etc.

In thiswork we will be designing DOCCCII in 16 nm bulk CMOS and discuss its features.

II. DUAL OUTPUT CURRENT CONTROLLED CURRENT CONVEYOR (DOCCCII)

After its introduction in 1995 [10] CCCII has been the first choice of analog designers mainly because it includes a X- node parasitic resistance which can be electronically controlled through the input bias current and so needs no additional resistance for activation. Current negation and current duplication is very easy to obtain in case of a CCCII, leading to DOCCCII. The equivalent circuit symbol and the principal equation of DOCCCII are given in Figure.1 and Equation 1. DOCCCII has two high impedance current output nodes which provide quadrature signals.

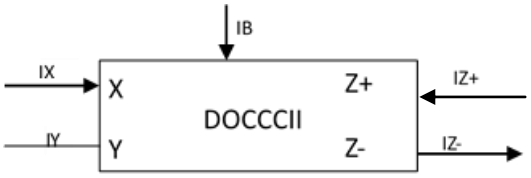

Figure 1. Block Diagram of DOCCCII

$$\begin{bmatrix} \mathrm{Vx} \\ Iy \\ Iz \pm \end{bmatrix} = \begin{bmatrix} Rx & 1 & 0 \\ 0 & 0 & 0 \\ +1 & 0 & 0 \end{bmatrix} \begin{bmatrix} Ix \\ Vy \\ Vz \end{bmatrix} \quad (1)$$

$$R_x = \frac{1}{g_{m2} + g_{m4}}$$

Where R_x is the parasitic internal resistance at port X and is controlled by bias current I_B.

The CMOS implementation of a class AB DOCCCII is presented in figure. 2. The circuit consists of a translinear loop consisting of transistors M1 – M4. Two MOS current mirrors (M5 – M6 and M7 – M8) are used to bias the translinear loop with bias current I_B, the input cell presents a high input impedance at input port *Y* and a low input impedance at input port *X*. This cell acts as voltage follower. The current at node *X* is copied to output nodes *Z*+ and *Z*–. Currents *Id18* and *Id14*are cross-coupled through transistors M14, M15, M18 and M19 to generate negative current at *Z*- node. Details are shown in the circuit given in figure 2.

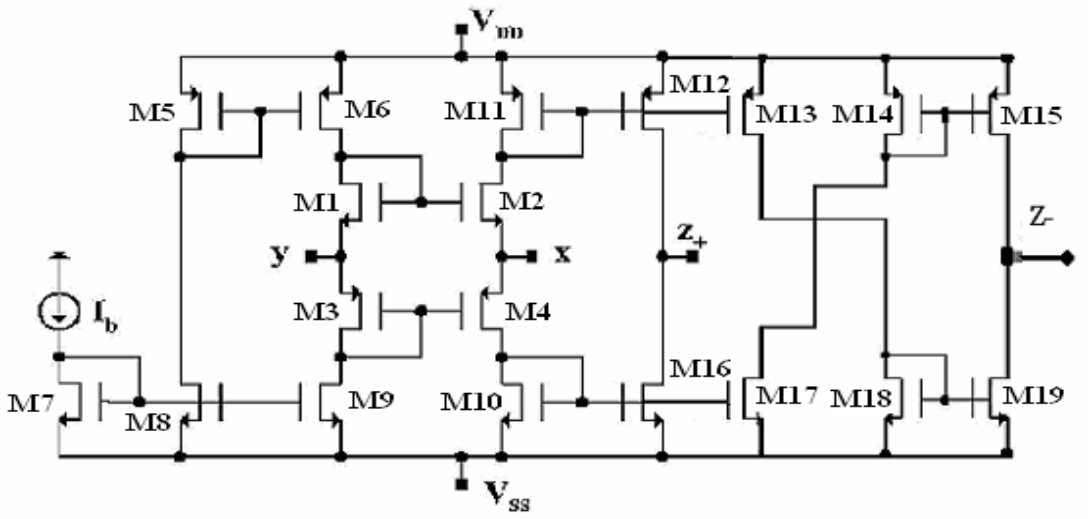

Figure 2 CMOS implementation of DOCCCII

III. RESULT AND DISCUSSION

The DOCCCII is designed and simulated in H-spice using 16nm bulk CMOS PTM [21] to validate its functionality. The figures3&4 shows the AC and transient analysis of DOCCCII. AC analysis gives the range of frequencies of operation. To study the signal processing capability of the DOCCCII transient analysis has been carried out with 1GHz frequency for sinusoidal input. It was observed from the analysisthat at frequencies higher than 1GHz there is a phase shift in the output, so its actual range of frequency is 1GHz. In figures5 and 6, R_X vs bias current variation and temperature stability of current gain of DOCCCII are shown respectively.

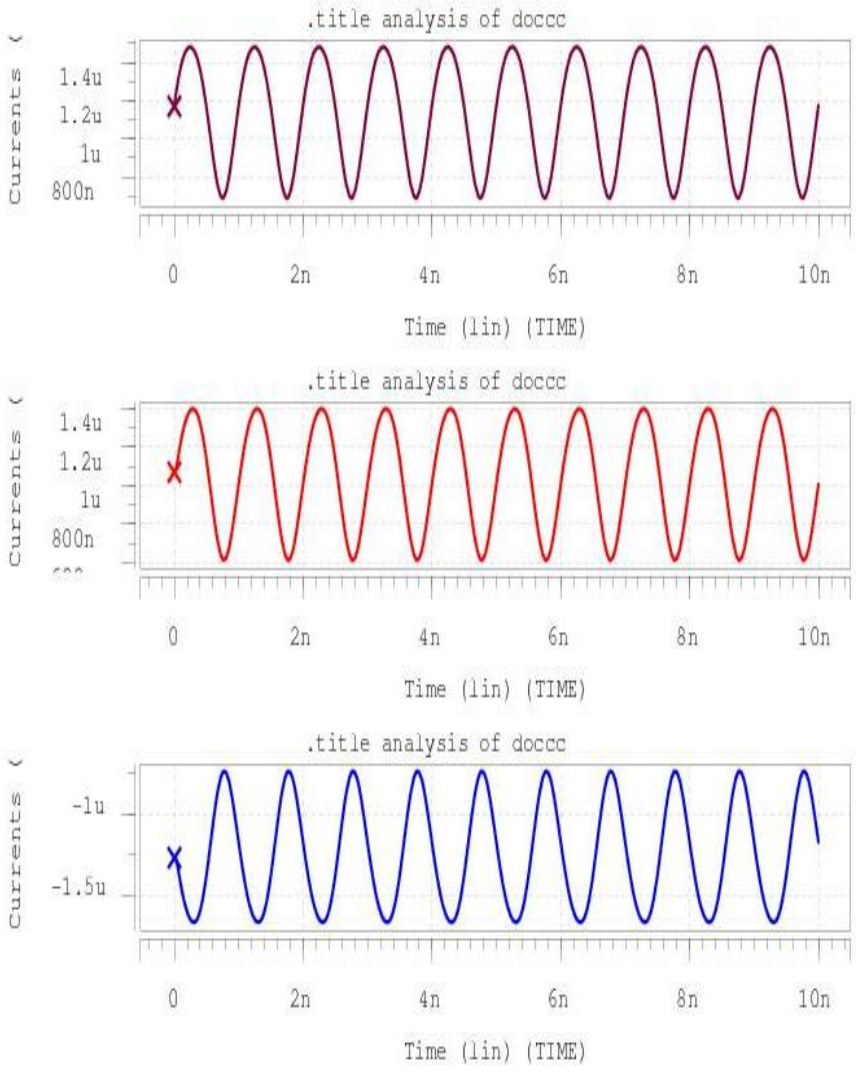

Figure 3: Transient Analysis of DOCCCII

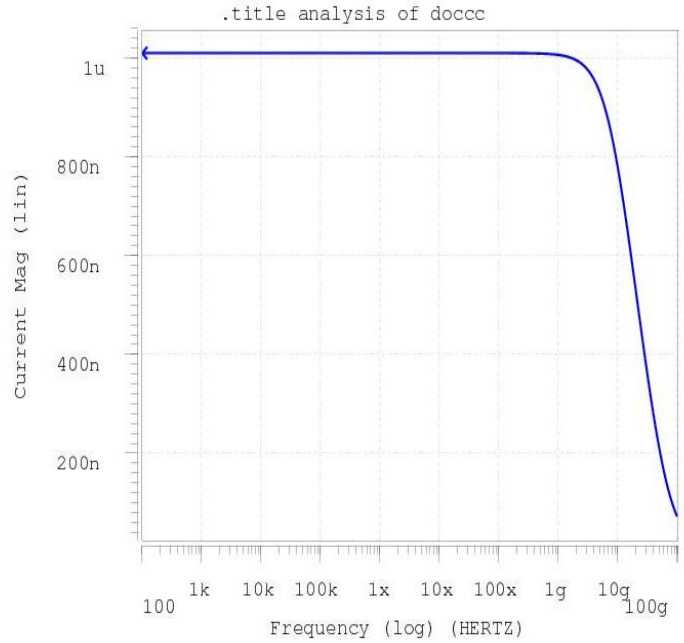

Figure 4: AC analysis of DOCCCII

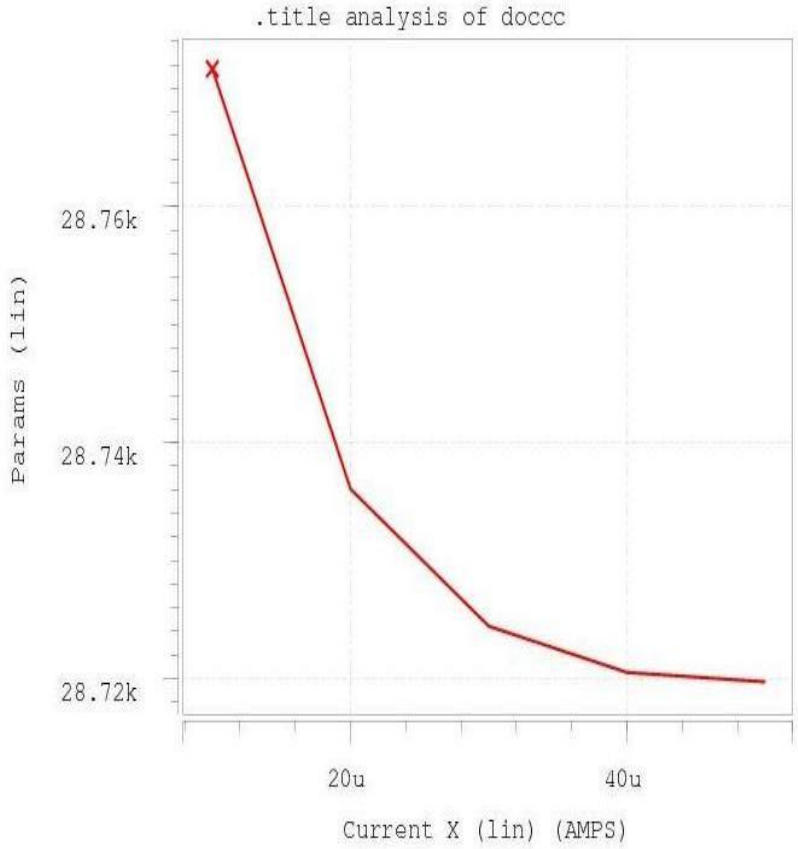

Figure 5: Rx versus bias current variation of DOCCCII

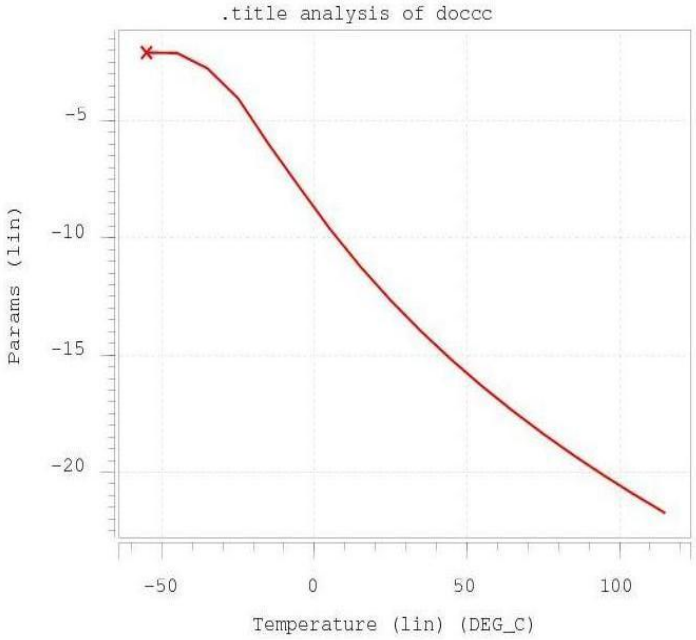

Figure 6: Temp stability of DOCCCII

Table 1: Performance parameters of DOCCCII

Supply voltage	0.7V
Current gain	1.0996
Bandwidth	12.2825GHz
Input resistance	32Kohm
Output resistance	574.236KΩ
Power dissipation	53.2503**µ**watts

IV. CONCLUSION

The DOCCCII is simulated and studied in 16 nm technology. The flexibility of programming the internal resistance can be used to synthesize variable gain filters and oscillators with tunable frequency, voltage and current amplifiers of varying gain. The DOCCCII can be used as a building block for field programmable analog array (FPAA).

REFERENCES

[1]. S. Sedra, *et al.*, "The Current Conveyor: History, Progress and New Results," IEE Proceedings (Part G) ofCircuits, Devices and Systems, Vol. 137, No. 2, April 1990, pp. 78-87. doi:10.1049/ip-g-2.1990.0015
[2]. Giuseppe Ferri and Nicola .C.Guerrinni, "Low voltage low power CMOS current conveyors", Print ©2003 Kluwer academic publishers, Dordrecht.
[3]. Giuseppe Palnisano, Gaetano Palumo, Salvatore Pennisi, "CMOS Current Amplifiers", Kluwer Academic publishers, 1999.
[4]. F. Yuan, "CMOS Current-Mode Circuits for DATA Communications", Springer Verlag, 2007.
[5]. C.H. Lee, J. Cornish, K. McClellan, J. Choma Jr., "Current-Mode Approach for Wide-Gain Bandwidth Product Architecture", IEEE Trans. Cir. Sys. II, Vol. 45, May 1998.
[6]. L.N. Alves, R.L. Aguiar, "A Differential Current-Conveyor Based Buffer for High-Bandwidth Low-Signal Applications", ICECS99, Paphos, Cyprus, Sep.
[7]. B. Wilson, "Recent developments in current conveyors and current mode circuits," IEE Proceedings-*G*, pp. 63 – 77, 1990
[8]. R. Senani, "Novel circuit implementation of current conveyors using an OA and an OTA," Electron. Lett. , vol. 16, no. 1, pp. 2–3, Jan. 1980.
[9]. B. Wilson, "Recent developments in current conveyors and current mode circuits," IEE Processing, Pt. G, vol. 137, pp. 63-77, April, 1990.
[10]. A.Fabre, O. Saaid, F. Wiest, and C. Baucheron, High frequency applications based on a new current controlled conveyor, IEEE Transactions. Circuits System-I, vol. 43,no. 2, pp. 82-90,
[11]. M.Y.Yasin, Bal Gopal "High Frequency Oscillator Design Using a Single 45 nm CMOS Current Controlled Current Conveyor (CCCII+) with Minimum Passive Components" Circuits and Systems,2011,2,53-59, doi:10.4236/cs.2011.22009
[12]. Pipat Prommee,Montri sondunyakanok, " CMOS based current controlled DDCC and its applications to capacitance multiplier and universal filter" Int.J.Commun.(AEU) 65 pp.1-8, 2011.

[13]. A. U. Keskin, D. Biolek, E. Hancioglu and V. Biolkova, Current-mode KHN filter employing current differencing transconductance amplifiers, Int'l J. Electronics and Comm. 60 (2006) 443-446
[14]. N. Herencsar, J. Koton and K. Vrva, Single CCTA-based universal biquad filters employing minimum components, Int'l J. Computer and Electrical Eng. 1307-310,(2009).
[15]. T. Thosdeekoraphat, S. Summart, C. Saetiaw, S.Sanatalunai and C. Thongsopa, Resistor-less currentmode universal biquad filter using CCTAs and grounded capacitors, World Academy Of Science, Eng. and Tec. 69 ,559-563, (2012).
[16]. S. V. Singh, S. Maheshwari and D. S. Chauhan, Universal current-controlled current-mode biquad filter employing MO-CCCCTAs and grounded capacitors, J.Circuits and Syst.1, pp.35-40. 2010
[17]. Winai jaikala, Montree Siripruchyanum, Phamorn Silapan, " Realization of CMOS Current Controlled Current Conveyor Transconductance Amplifier CCCCTA and Its Applications" J. of Active and Passive Electronics Devices,Vol.4,pp.35-40,2009.
[18]. Sajai Vir Singh,Sudhanshu Maheshwari "Current-Processing Current-Controlled, Universal Biquad Filter",Radio Engineering,Vol.21,no1, April 2012
[19]. Iqbal.A.Khan,Ahmed.M.Nahhas, "Current Mode Programmable Analog Modules using Low voltage .Digitally Controlled CMOS CCII", International Journal Of Computer applications(0975-888),vol.48,no4,June 2012
[20]. T.M. Hassan,S.A.Mahmoud,"New CMOS Digitally Controlled Variable Gain Aplifier" International Conference On Microelectronics, 2008.
[21]. Predictive Technology Model, 2006 http://ptm.asu.edu.