International Journal of Research in Engineering and Science (IJRES)
ISSN (Online): 2320-9364, ISSN (Print): 2320-9356
www.ijres.org Volume 10 Issue 12 ǁ December 2022 ǁ PP. 312-318

Design of Current Mode SIMO Filter using VD-DXCC

[1]Vinod Kumar Yadav, [1]Sanjay Chauhan, [1]Umesh Singh
[1]*Department of Electronics and communication Engineering, Institute of Engineering and Technology, Dr. Ram Manohar Lohia Avadh University, Ayodhya, India*
Corresponding Author:vinod.ece07@gmail.com

Abstract
Advancement in VLSI technology has led to largernumber of components on a single chip making it a reality to realizeportable systems. Analog circuits are important in every VLSI systemsuch as filters, current and voltage amplifiers, comparators, A/D andD/A converters, etc. Miniaturization in circuit design requires lowpower low-voltage (LPLV) analog integrated circuits to be designed.Analog signal processing's inherent advantage of low power and highspeed has led to extensive research in analog domain. Current domainprocessing having advantages of higher bandwidth, large dynamicrange, greater linearity, simple circuitry seems to be the solution.Among the number of current mode topologies current conveyor is themost versatile building block. A current mode active block the voltage differencing dual x current conveyor (VD-DXCC) is designed using floating gate technique. The designed VD-DXCC is used for the design of current mode single input multiple output (SIMO) filter. The filter can output all five filter responses high pass, low pass(LP), band pass(BP), band reject(BR) and all pass(AP). The analysis is done using 0.18µm CMOS technology using Spice software.

Keywords: *Analog circuits, Current mode, Current conveyor, Signal processing*

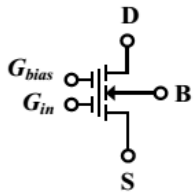
Date of Submission: 06-12-2022 Date of acceptance: 18-12-2022

I. INTRODUCTION

Filters are an integral part of almost every electronicsystem and so their synthesis and developmentremain an ever-evolving field. Among various filterstructures universal filters are the most versatile as allthe standard filter functions can be derived from them[1]. They serve as standalone solution to manyfiltering needs.Owning to their inherent advantage of widebandwidth, high slew rate, low power consumption,simple circuitry, and excellent linearity [2-3] currentconveyors (CC) are widely used in electronic design.Moreover, the requirement of low voltage low poweroperation put forward by portable electronic devicesand the energy harvestingsystems [4-5] etc. furtherencourages the use of CC. The current controlledcurrent conveyor (CCCII) is the most versatile activeelement due to its electronically tunable parasiticresistance [6]. Numerous filter implementationsutilizing CCCII can be found in the open literature[6]. The universal filter structure can be regarded asthe most flexible as it can realize all the standardfilter functions without any alteration in its topology.In the present-day mixed mode design environmentwhere many systems interact many times the needarises for the current mode and voltage mode circuitsto be connected. This requirement can bemet by employing trans-admittance mode (TAM) andtrans-impedance mode (TIM) filter structures whichcan serve as the interface providing distortion freeinteraction. Although several TAM and TIMfilter structures can be found in the literature [7] but asingle topology providing the CM, VM, TAM andTIM responses will be an added advantage in termsof area and power requirements. In the past twodecades, anumber of mixed mode filters have beenproposed utilizing different current mode activeelements like dual output current controlled currentconveyor (DOCCCII), multi output current conveyor(MOCCII) [6], current controlled current conveyortransconductance amplifier (CCCCTA) [6], Currentfeedback operational amplifiers (CFOA) [6], fullydifferential current conveyor (FDCCII) [6],differential difference current conveyor and digitallyprogrammable current conveyor (DPCCII)[6]etc.Many reported universal structures useseveral active and passive elements like the onereported by [9] with six CCII, oneDOCCII,eight resistors and two grounded capacitors.The filter is able to realize all filter function in four modes. The same author [10] presented anothermixed mode universal filter employing fourDOCCCII and two capacitors. Although the activeand passive elements are halved compared to theprevious design but still the structure was not able torealize all pass response in any mode. The author in [11] proposed single input multi output (SIMO)filter employing three CCCCTAs and two groundedcapacitors. The circuit is capable of realizing HP, LPand BP responses in all four modes. Additionally, thefilter can realize low pass notch (LPN), high passnotch (HPN) and AP responses in CM and TAMmodes of operation. The author in [12]proposed a CM and TIM mode nth order filter usingMOCCII realizing all standard filter functions. Thefilter required (n+1) MOCCII, (n+1) resistors and ngrounded capacitors for realization. For therealization of second order response the filterstructure would require three MOCCII, three resistorsand three capacitors which will result in large areaand increased power dissipation. The

author in [13] proposed a CM and VM mode universal filterrealizing all standard functions in both the modes.The multi input single output (MISO) structureemploys two DOCCCII and two capacitors. The circuit also has the independent tuning capability.The author in [14] presented a mixed mode universalfilter employing one DOCCCII, one MOCCCII, tworesistors and two capacitors. The circuit is capable ofrealizing all the standard filter functions in the fourmodes with electronic tunability.

With the increased advancement in miniaturized circuits that can perform specialized tasks like portable activity monitors, smart watches, electrocardiogram (ECG) machines, smart phones and blood pressure monitors etc. The requirement to prolong the battery life span of the devices has increased. These smart battery-operated devices pose four major challenges for the designers. First, longer battery life span, low voltage operation, higher transistor packing density and high operational speed. Since it is not possible to achieve each of the above requirements independently a good tradeoff between the parameters need to be achieved. To achieve performance enhancement and ultra-high packing density aggressiveComplementary Metal Oxide Semiconductor (CMOS) scaling is done. This led to rapid shrink in size of the semiconductor devices, high speed, reduction in supply voltage and reduced power dissipation. This scaling proved beneficial for the digital designs but resulted in severe performance degradation for analog design. The major reason for this is that the threshold voltage cannot be scaled in the same ratio as the supply voltage and so it takes up a substantial fraction of the total supply voltage leading to decreased dynamic range and bandwidth. To mitigate this problem novel techniques have been developed which can be categorized in two main levels. First, circuit level design technique which includes adopting numerous circuit level techniques to achieve high performance designs like folded cascode, class AB stage, level shifting, subthreshold operation, self cascode and composite transistor. Recently, researchers also utilized special connection of metal oxide semiconductor (MOS) transistor to remove or reduce threshold voltage from signal path [18]. These include floating gate MOS (FG-MOS), bulk driven MOS (BD-MOS) and dynamic threshold MOS (DTMOS) techniques [18-19]. The FGMOS technique involves leaving the gate electrode floating; two or more control gates are formed over this electrode using a second polysilicon layer deposition. Figure 1 (a) presents the symbol of a two-input NMOS Floating-Gate transistor. The equivalent circuit is shown in Figure (b). The voltage at the floating gate is given by Equation 1.



(a) (b)

Figure 1:(a) The symbol of FG-MOS (b) Equivalent circuit of FG-MOS

$$V_{FG} = \frac{C_{in}V_{in}+C_{bias}V_{bias}+C_{GD}V_D+C_{GS}V_S+C_{GB}V_B+Q_{FG}}{C_{Total}} \quad (1)$$

Where Q_{FG} is the residual charge trapped at the FGMOS during the fabrication process. The total capacitance $C_{Total} = C_{in} + C_{bias} + C_{GD} + C_{GS}+C_{GB}$, where C_{GD}, C_{GS}, C_{GB} are the parasitic capacitances associated with the source, drain and bulk region respectively. If the input capacitance is selected such that their sum is much greater than the parasitic capacitances, then voltage on floating gate is given by Equation 2.

$$V_{FG} \approx K_1V_{in} + K_2V_{bias} \quad (2)$$

Where $K_1 = \frac{C_{in}}{C_{Total}}$ and $K_2 = \frac{C_{bias}}{C_{Total}}$ are the equivalent weights. The equivalent threshold voltage of FG-MOS is given by Equation 3.

$$V_{Threshold-FG} = \frac{V_T - V_{bias}K_2}{K_1} \quad (3)$$

Where V_T is the threshold voltage of a conventional gate driven MOS(GD-MOS) transistor. It can be deduced from the equation that by suitable choice of K_1, K_2 and V_{bias} the threshold voltage of the FG-MOS can be reduced or made zero.

In thiswork we have used floating gate technique to design a recently presented building block the voltage differencing dual X current conveyor (VD-DXCC). The LV VD-DXCC in further used in the design of current mode single input multi output (MISO) filter.

II. Voltage Differencing Dual X Current Conveyor (VD-DXCC)

The Voltage Differencing Dual X Current Conveyor (VD-DXCC) [20] is functionally a connection of DXCCII and OTA. The new block carries features of inverting current conveyor (ICCII), CCII, and tunable trans-conductor in one single architecture which is also simple to implement and develop into integrated circuit. The Voltage current characteristics of the developed VD-DXCC are given in matrix Equation 4 and the block diagram is presented in Figure. 2.

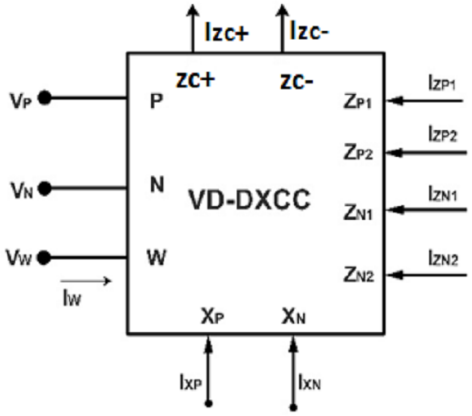


Figure 2: Block diagram of VD-DXCC

$$\begin{bmatrix} I_N \\ I_P \\ I_{zc\pm/I_W} \\ V_{XP} \\ V_{XN} \\ I_{ZP1} \\ I_{ZP2} \\ I_{ZN1} \\ I_{ZN2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_W \\ I_{XP} \\ I_{XN} \\ V_{ZP1} \\ V_{ZP2} \\ V_{ZN1} \\ V_{ZN2} \end{bmatrix} \quad (4)$$

To realize low voltage operation floating gate techniques is used for the implementation. The input transistors (M1-M2) and (M13-M17) are realized using FG-MOS technique. The CMOS implementation of VD-DXCC is presented in Figure 3.9. It is a eight-terminal active element. The second stage consists of DXCCII, transistors (M13-M32). The voltage at W appears at V_{XP} and in inverted format atV_{XN}. The current input at X_p node is transferred to nodes Z_{P1}andZ_{P2}. In the same way the current from X_N node is transferred to $Z_{N1}$and Z_{N2}. The W and Z nodes are high impedance while the X_P and X_N node are low impedance.The First stage is composed of OTA. The transconductance is realized using transistors (M1-M2). The output current of the trans-conductor depends on the voltage difference between voltages at terminals P and N. Assuming saturation region operation for all transistors and equal W/L ratio for transistors M1 and M2 the output current $I_{ZC+}, I_{\boldsymbol{ZC-}}$ of the OTA is given by Equation 5.

$$I_{\boldsymbol{ZC+}} = -I_{\boldsymbol{ZC-}} = g_m(V_P - V_N) = \left(\sqrt{2I_{Bias}\,k}\right)(V_P - V_N) \quad (5)$$

Where, the transconductance parameter $K_i = \mu C_{ox} {}^{W}/_{2L}$ $(i = 1, 2)$, W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area and μ is the carrier mobility. It is evident from (3.26) that the transconductance can be tuned by the bias current thus imparting tunability to the structure.

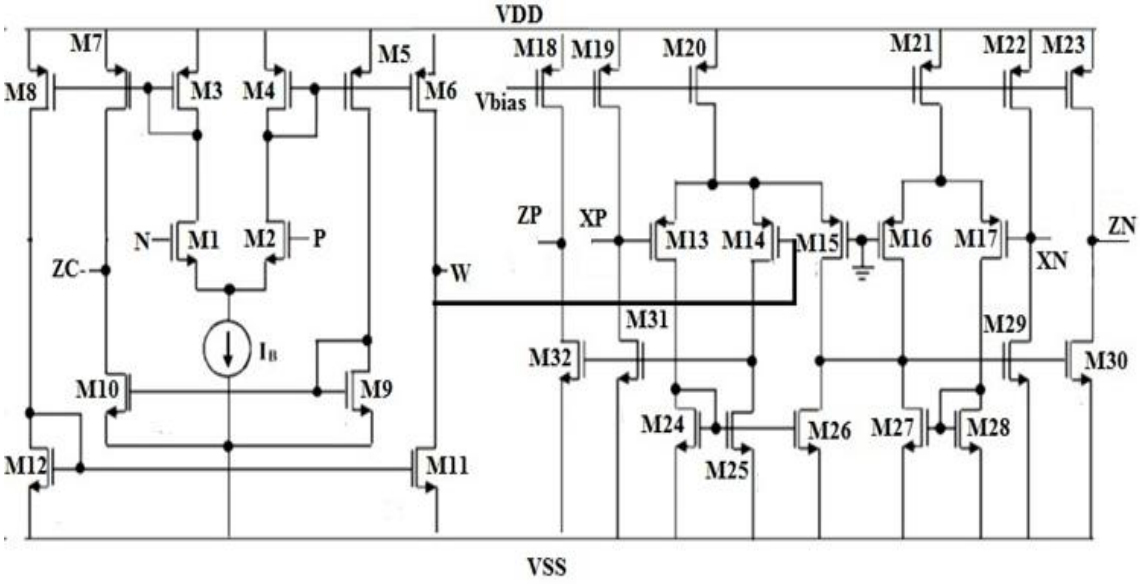


Figure Error! No text of specified style in document.**:CMOS Implementation of VD-DXCC**

III. Current Mode Filter

The SIMO filter structure is shown in Figure 4. The filter employs single VD-DXCC and two resistors and two capacitors for implementation. This topology has additional output terminals to provide explicit current output from high impedance nodes. The filter transfer function and expression for pole frequency and quality factor are summarized in Equations 6 until 10. The CM filter can provide LP, HP, BP, BR and AP responses simultaneously.

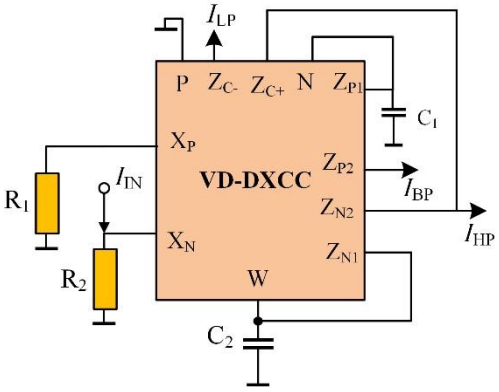


Figure 4:SIMO filter structure

$$\frac{I_{HP}}{I_{IN}} = -\frac{S^2C_1C_2R_1R_2}{S^2C_1C_2R_1R_2 + sC_2R_1 + R_2g_m} \tag{6}$$

$$\frac{I_{LP}}{I_{IN}} = -\frac{g_mR_2}{S^2C_1C_2R_1R_2 + sC_2R_1 + R_2g_m} \tag{7}$$

$$\frac{I_{BP}}{I_{IN}} = -\frac{sC_2R_1}{S^2C_1C_2R_1R_2 + sC_2R_1 + R_2g_m} \tag{8}$$

$$\omega_o = \sqrt{\frac{g_m}{C_1 C_2 R_1}} \tag{9}$$

$$Q = R_2 \sqrt{\frac{g_m C_2}{C_1 R_1}} \tag{10}$$

IV. RESULT AND DISCUSSION

To validate its functionality the VD-DXCC is designed in 0.18µm technology using Spice software at a supply voltage of ±0.9 V. The width and length of the transistors used are given in Table 1. The bias current of the OTA is fixed at 80µA resulting in transconductance of 756µS.

Table 1: Width and Length of the MOS transistors

Transistors	Width (µm)	Length (µm)
M1-M2, M5-M6	2.8	0.36
M3-M4, M7-M9	5.8	0.36
M10-M14	1.8	0.72
M15-M18	.06	0.36
M19-M22	4	0.36
M23, M25, M27, M33, M42, M44	2.16	0.36

To verifythe CM mode SIMO filter,it is designed for a frequency of 5.408 MHz. The passive elements are selected as $R_1 = 4k\Omega$, $R_2 = 4k\Omega$, $C_1 = 10pF$, $C_2 = 10pF$ and I_{Bias}=20uA. The response of the filter is shown in Figures 5. The quality factor tunability is also tested for different values of the resistor R_2 as presented in Figure 6. It can be inferred from the figure that the quality factor can be tuned independent of the frequency. The transient analysis result for BP configuration is also presented in Figure 7 which further testifies the accurate signal processing capability of the filter structure. The transient analysis is done by applying a sine wave of 5.4MHz frequency and 30µA p-p current amplitude.

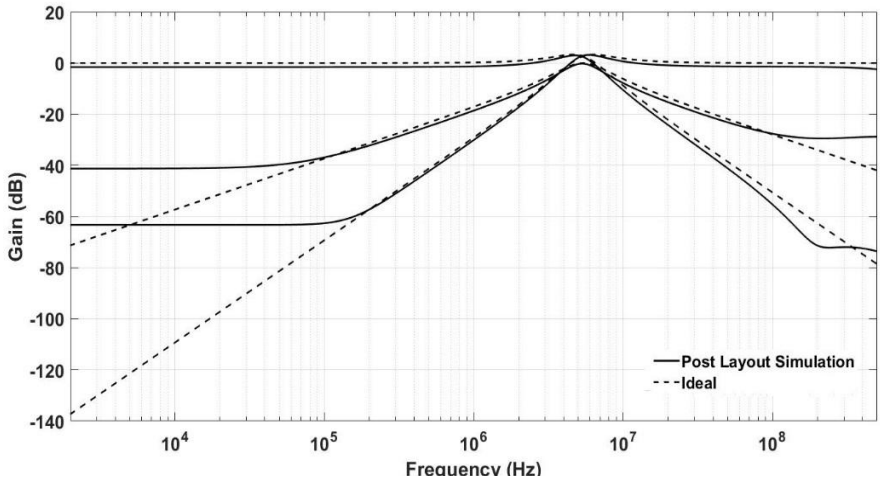


Figure 1:Frequency response of CM SIMO Filter

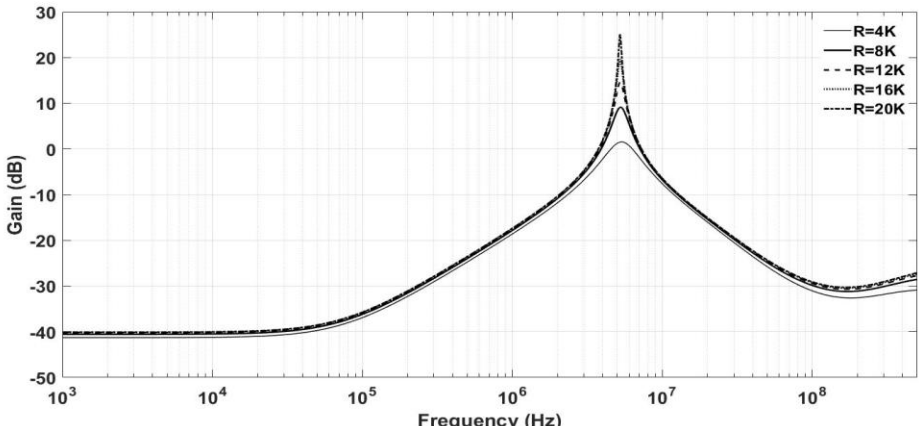


Figure2:Quality factor tunability of CM SIMO Filter

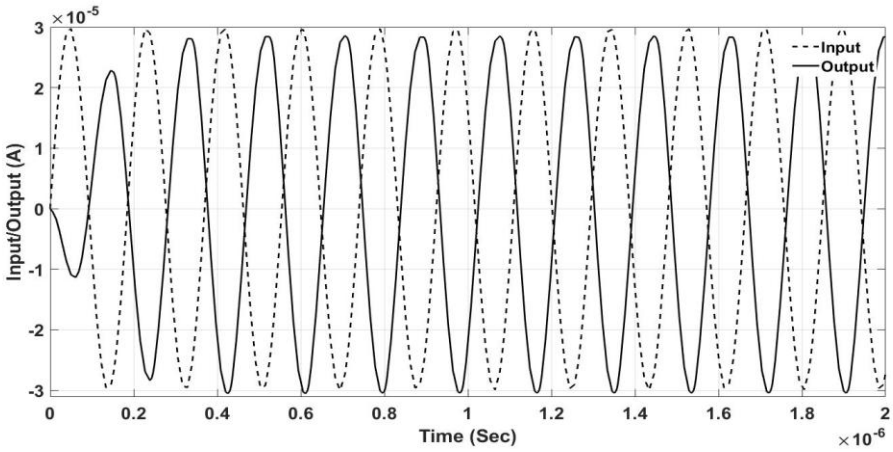


Figure 3:Transient analysis of BP SIMO filter configuration

The Monte Carlo analysis is carried out for the CM SIMO filter for 10% variation in resistors (R_1&R_2) values for BP response. The analysis is done for 200 runs and the results are presented in Figures 8. Additionally, Monte Carlo analysis is also done for 10% variation in capacitors (C_1&C_2) values. The results are given in Figure 9. It can be inferred from the analysis results that the filter does not require any passive components matching constraints.

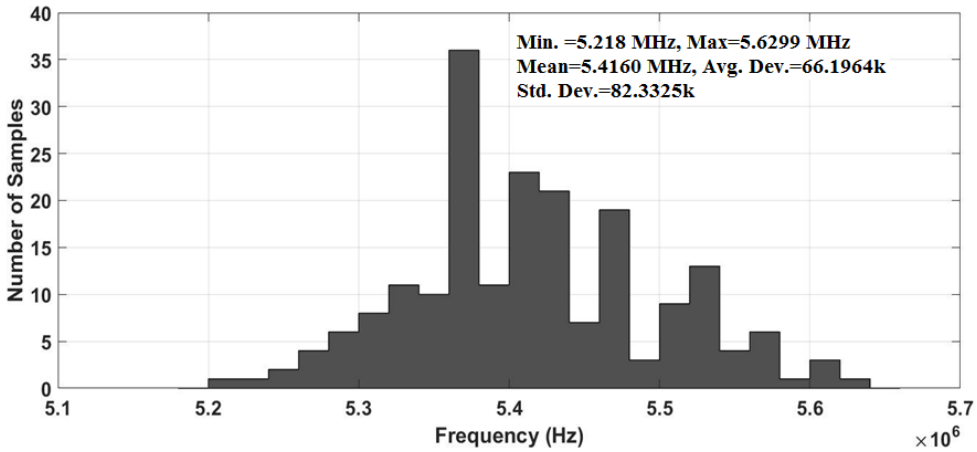


Figure4:The Monte Carlo analysis results for BP response

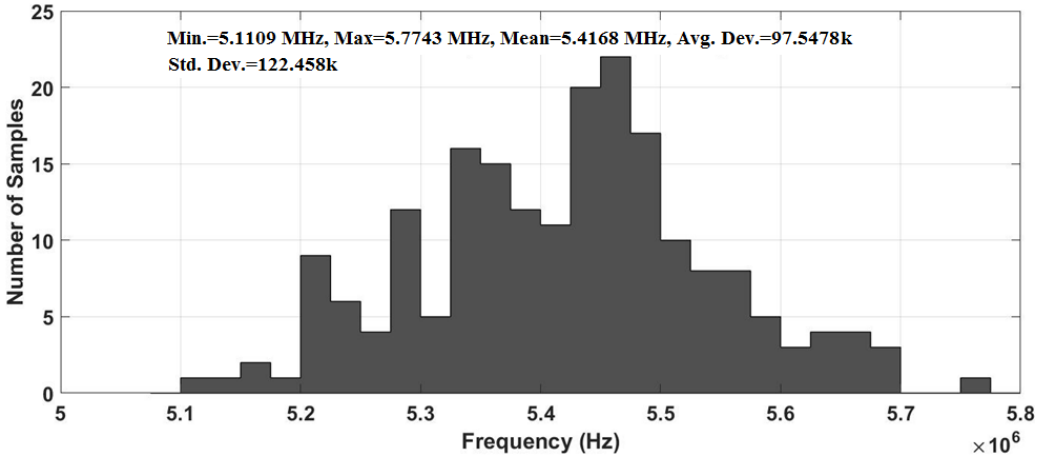


Figure5:The Monte Carlo analysis results for BP filter response

V. CONCLUSION

A current mode SIMO filter is designed using low voltage low power VD-DXCC active block. The floating gate technique is used for the design of LV VD-DXCC. The designed filter uses two grounded resistors, two capacitors and single VD-DXCC for implementation. The filter can provide all filter function simultaneously with any passive component matching. The filter is designed for a frequency of 5.4MHz and tested using Spice software.

REFERENCES

[1]. Horng, J. W. (2001). High-input impedance voltage-mode universal biquadratic filter using three plus-type CCIIs. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, *48*(10), 996-997.

[2]. Sedra, A. S., Gordon W. Roberts, and F. Gohh. (1990) "The current conveyor: history, progress and new results." In *IEE proceedings*, vol. 137, no. 2, pp. 78-87.

[3]. Toumazou, C., Lidgey, F. J., & Haigh, D. (Eds.). (1990). *Analogue IC design: the current-mode approach* (Vol. 2). Presbyterian Publishing Corp.

[4]. Sampe, J. A. H. A. R. I. A. H., Zulkifli, F. F., Semsudin, N. A. A., Islam, M. S., & Majlis, B. Y. (2016). Ultra low power hybrid micro energy harvester using rf, thermal and vibration for biomedical devices. *International Journal of Pharmacy and Pharmaceutical Sciences*, *8*(2), 18-21.

[5]. Faseehuddin, M., Sampe, J., & Islam, M. S. (2016). Designing ultra low voltage low power active analog blocks for filter applications utilizing the body terminal of MOSFET: A review. *Asian Journal of Scientific Research*, *9*(3), 106-121.

[6]. Senani, R., Bhaskar, D. R., & Singh, A. K. (2015). *Current conveyors: variants, applications and hardware implementations* (Vol. 560). Switzerland: Springer International Publishing.

[7]. Minaei*, S., Topcu, G., & Cicekoglu, O. (2005). Low input impedance trans-impedance type multifunction filter using only active elements. *International journal of electronics*, *92*(7), 385-392.

[8]. Yasin, M. Y., & Gopal, B. (2011). High frequency oscillator design using a single 45 nm CMOS current controlled current conveyor (CCCII+) with minimum passive components. *Circuits and systems*, *2*(02), 53.

[9]. Abuelma'atti, M. T. (2003). A novel mixed-mode current-controlled current-conveyor-based filter. *Active and passive electronic components*, *26*(3), 185-191.

[10]. Abuelma'atti, M. T., Bentrcia, A., & Al-Shahrani, S. A. M. (2004). A novel mixed-mode current-conveyor-based filter. *International Journal of Electronics*, *91*(3), 191-197.

[11]. Maheshwari, S., Singh, S. V., & Chauhan, D. S. (2011). Electronically tunable low-voltage mixed-mode universal biquad filter. *IET circuits, devices & systems*, *5*(3), 149-158.

[12]. Horng, J. W. (2009). High-order current-mode and transimpedance-mode universal filters with multiple-inputs and two-outputs using MOCCIIs. *Radioengineering*, *18*(4), 537-543.

[13]. Siripruchyanun, M., & Jaikla, W. (2007). Three-input single-output electronically controllable dual-mode universal biquad filter using DO-CCCIIs. *Active and Passive Electronic Components*, *2007*.

[14]. Pandey, N., Paul, S. K., Bhattacharyya, A., & Jain, S. B. (2010). Realization of Generalized Mixed Mode Universal Filter Using CCCIIs. *Journal of Active & Passive Electronic Devices*, *5*.

[15]. Zhijun, L. (2009). Mixed-mode universal filter using MCCCII. AEU-International Journal of Electronics and Communications, 63(12), 1072-1075.

[16]. Senani, R. (2005). Novel mixed-mode universal biquad configuration. IEICE Electronics Express, 2(22), 548-553.

[17]. Horng, J. W. (2011). High output impedance current-mode universal biquadratic filters with five inputs using multi-output CCIIs. Microelectronics Journal, 42(5), 693-700.

[18]. Khateb, F., Khatib, N., & Kubánek, D. (2012). Novel ultra-low-power class AB CCII+ based on floating-gate folded cascode OTA. *Circuits, Systems, and Signal Processing*, *31*(2), 447-464.

[19]. Varun, N. (2016). A novel low power FGMOS-CCII based fully CMOS four quadrant multiplier. In *2016 International Conference on Computing, Communication and Automation (ICCCA)* (pp. 1377-1381). IEEE.

[20]. Albrni, M. A., Faseehuddin, M., Sampe, J., & Ali, S. H. M. (2019). Novel dual mode multifunction filter employing highly versatile VD-DXCC. *Informacije MIDEM*, *49*(3), 167-176.