International Journal of Research in Engineering and Science (IJRES)
ISSN (Online): 2320-9364, ISSN (Print): 2320-9356
www.ijres.org Volume 1 Issue 7 ǁ Nov. 2013 ǁ PP.23-29

AVTS Approach To Digital CMOS Circuits For Diminishing Complete Power Expenditure

[1]S.Hari Prasath Sharma, [2] G.Vishnu Sankar,[3] S.M.K.Srikanth, [4] Dharitri Ray
[1]PG Scholar Technology of VLSI Design, [2] PG Scholar Technology of Embedded Systems
[3] PG Scholar Technology of Embedded Systems, [4] PG Scholar Technology of VLSI Design
(Department of Electronics and Communication Engineering, Bharath University-Chennai, India)

ABSTRACT:
Power utilization of present Digital integrated circuits escalating with each generation which becomes a serious design issue. This paper wished-for a generalized power tracking algorithm that reduces power directly by forceful control of supply voltage and body bias. The AVTS algorithm-(Active Voltage and Threshold Scaling algorithm) save the outflow power for the period of Active mode of the circuit. Total Active power can be diminishing by adjusting Vdd and Vth based on circuit operating environment such as hotness, operation load, and circuit structural design. The power saving method of AVTS is similar to that of the Active Voltage Scaling (AVS) scheme, which adaptively changes the supply voltage depending on the current function of the system. For the circuits, and it is possible to trade off active and sub threshold outflow power by balancing between Vdd and Vth to maintain performance

Keywords - Active Voltage and Threshold Scaling (AVTS), Active Voltage Scaling (AVS) scheme, Leakage Current Control, Low Power, Power finest Point

I. INTRODUCTION

Low power has emerged as a most important argument in today's electronics engineering industries. They require low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. In the past, the major concern of the VLSI designer was area, performance, price and consistency; power contemplation was secondary significance. In current days, however, this has begun to change and, increasingly, power is being given similar weight to area and speed considerations. Several factors have contributed to this fashion. possibly the most important driving factor has been the significant success and extension of the class of individual computing strategy (portable desktops, audio- and video-based multimedia goods) and wireless communications systems (personal digital assistants and special communicators) which demand express computation and complex functionality with low power utilization.

Power dissipation has become an important objective in the design of digital circuits. There has been intense research over the past two decades on various aspects of compilation and synthesis for low power. Many architectural optimizations like re-configurable architectures, custom ASIC approaches, programmable multi-cores, *etc*... Micro- architectural method like parallelism and pipelining, power and clock gating has become common place now. Circuit techniques for low voltage operation, reserve current decrease, finest gate sizing have also been explored and are available for use by a designer. Most of these optimization techniques are static techniques which are applied during design time. In the recent past, Active power management techniques have emerged, where the power consumption is continuously adjusted during run time of the system.

Traditionally, Active power management (DPM) is employed at operating system level to adjust the supply voltage for each power state. The supply voltage is conservatively margined to account for process and temperature variations. These voltage margin increases with technology scaling due to larger process variations, rendering DPM less efficient. On the other hand, the hardware approach like Active voltage scaling (AVS) allows voltage to be scaled such that the actual delay of the chip instead of worst case delay meets the target performance. This enables more power savings as minimum possible voltage for target performance can be attained. In AVS the supply voltage is adjusted to meet the target delay using an on-chip delay monitor in a hardware feedback loop. Performance degradation is a direct consequence of supply voltage reduction. In order

to maintain the required throughout, Active voltage scaling (AVS) systems are used to adjust the supply voltage according to throughput requirements. Though AVS very well manages the Active switching power, with shrinking feature size the static (leakage) power has increased exponentially which it cannot control. Particularly, at low activity levels, leakage power is dominant.

We present a Active VTH Scaling (AVTS) scheme to save the leakage power during Active mode of the circuit. Active Voltage and Threshold Scaling (AVTS) manages both Active and leakage powers by adjusting supply voltage and body bias voltage. The power saving strategy of AVTS is similar to that of the Active VDD Scaling (AVS) scheme, which adaptively changes the supply voltage depending on the current workload of the system. Instead of tuning the supply voltage, AVTS controls the threshold voltage by means of body bias control, in order to decrease the outflow power. The power saving potential of AVTS and its impact on Active and outflow power is applied to future technologies.

II. ACTIVE VOLTAGE AND THERSHOLD SCALING (AVTS)

Active Voltage and Threshold Scaling (AVTS) manages both Active and leakage powers by adjusting supply voltage and body bias voltage in digital circuits designed below 0.1 m, total power at any given performance can be optimized by AVTS. AVTS has been successfully proven on silicon for low power high speed applications. The optimum power point varies strongly with activity and temperature.AVTS offers considerable power savings compared to AVS when leakage power is a large fraction of total power. The power savings increase with increasing logic depth. The moderate performance application-specific integrated circuit (ASIC) with long logic depth at low activity and/or high temperatures gain the most with AVTS.

2.1 OVERVIEW OF AVTS

Active Vth Scaling (AVTS) scheme for Active leakage power reduction. Whenever there is a slack during computation, the Vth is adaptively changed to a higher value via changing the body bias voltage (VBB). This will deliver just enough amount of throughput required for the current workload. In order to examine the effectiveness of AVTS, comparisons between AVS and AVTS for current (0.25μm) and future (0.07μm) process generations are performed. A careful investigation on the advantages and disadvantages of AVTS over AVS is also made.

AVTS hardware that has a feedback loop consisting of a voltage controlled oscillator (VCO), charge pumps a feedback controller is proposed. The clock frequency of the system for a certain workload is determined by the operating system in run-time. The AVTS hardware tracks the optimal Vth for the given clock frequency by actively adjusting the VBB.

The AVTS scheme adaptively controls the body bias to change the Vth. For a time period when the workload is less than the maximum, the operating system will recommend a lower clock frequency to the hardware. Then the AVTS hardware will increase the PMOS body bias and decrease the NMOS body bias to raise the Vth and decrease power dissipation. The Vth can be increased as much as the upper limit of VBB, to significantly save the standby leakage power.

Reducing the clock frequency will proportionally reduce the total power. However, simply reducing the clock rate does not affect the energy consumed per operation. Whereas by scaling the supply voltage together with the frequency, we can gain significant power savings. This is because the Active power dominates the total power. Scaling the threshold voltage instead of scaling the supply voltage saves mostly the leakage power. For 0.25μm technology where the leakage power is a minute portion of the total power, AVTS is less efficient than AVS in saving total power.

2.2 MODULES OF AVTS SYSTEM

VDD CONTROLLER

- Vdd is the power supply to the digital circuit. Vdd will be scaled according to power consumption and time delay Maximum time delay will be set and between in that limits Vdd will be scaled.
- If Vdd goes below the minimum Vdd value Vdd value will be increased.

VBS CONTROLLER

- Vbs is the voltage between source and substrate. Vbs will effect threshold voltage .Vbs of the digital circuit will be varied to decrease the threshold voltage.
- In AVS only Vdd will be scaled to decrease total power consumption. In AVTS approach both Vdd and Vbs will be scaled to decrease total power consumption.

2.3 AVTS SCHEME

Active Vth Scaling (AVTS) scheme for Active leakage power reduction. Whenever there is a slack during computation, the Vth is adaptively changed to a higher value via changing the body bias voltage (VBB). This will deliver just enough amount of throughput required for the current workload. In order to examine the effectiveness of AVTS, comparisons between AVS and AVTS for current (0.25µm) and future (0.07µm) process generations are performed.

A careful investigation on the advantages and disadvantages of AVTS over AVS is also made. AVTS hardware that has a feedback loop consisting of a voltage controlled oscillator (VCO), charge pumps a feedback controller is proposed. The clock frequency of the system for a certain workload is determined by the operating system in run-time. The AVTS hardware tracks the optimal Vth for the given clock frequency by dynamically adjusting the VBB.

3.1 AVTS CONTROLLER

Fig.3.1 shows block diagram of close loop AVTS system. AVTS controller implements the proposed AVTS algorithm and controls the supply voltage regulator and well bias charge pump. Control signal generator (CSG) generates control signals for power monitor when START signal is asserted. The proposed AVTS system is suited for load circuits where the rate of change in activity is gradual. AVTS controller implements the proposed. AVTS algorithm and controls the supply voltage regulator and well bias charge pump. The drain of sleep transistor acts as a virtual ground node for the load circuit.

The power monitor processes virtual ground voltage to generate a 2 bit output that gives information on total power consumed by the load. Control signal generator (CSG) generates control signals for power monitor when START signal is asserted. The delay monitor measures whether performance of load circuit meets the target performance within tolerance limit. Delay monitor is implemented with a critical path replica circuit. The proposed AVTS system is suited for load circuits where the rate of change in activity is gradual. The maximum rate of change of activity that can be supported is discussed.

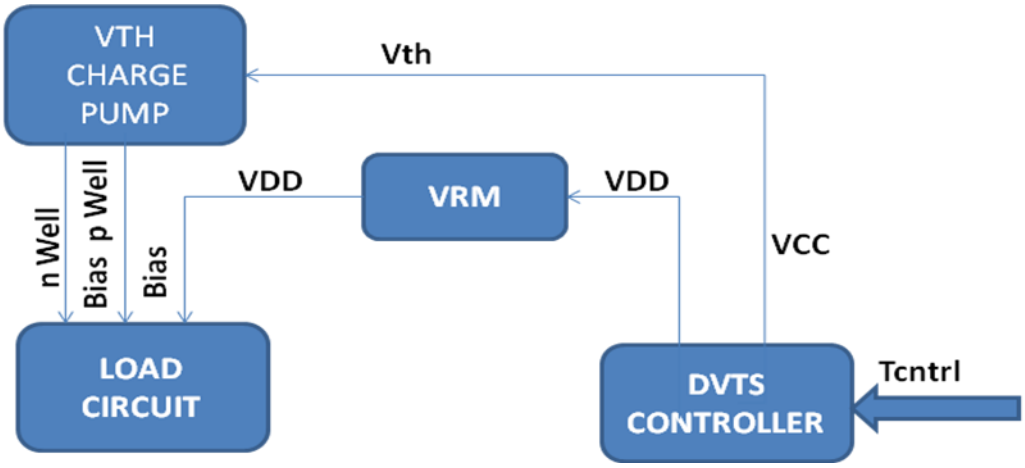

Fig.3.1 Design Implementation Block Diagram

3.2 AVTS ALGORITHM

Fig3.2. shows the flow chart of the proposed AVTS algorithm. The algorithm first sets the supply voltage to meet target performance, and then adjust well potential to achieve minimum power. Nwell bias and P Well bias are always tuned by same amount and hence AVTS control loop is essentially a 2-D control loop. To avoid oscillations, loop and loop are decoupled by tuning them independently. Initially maximum supply voltages and maximum forward bias are applied and the supply voltages are slowly lowered. At each step, the body bias is reset to maximum forward bias and locks to the target frequency to ensure that the chip stays functional. Once the smallest power point is discover, the bias values can be held in a register and the controller turned off.

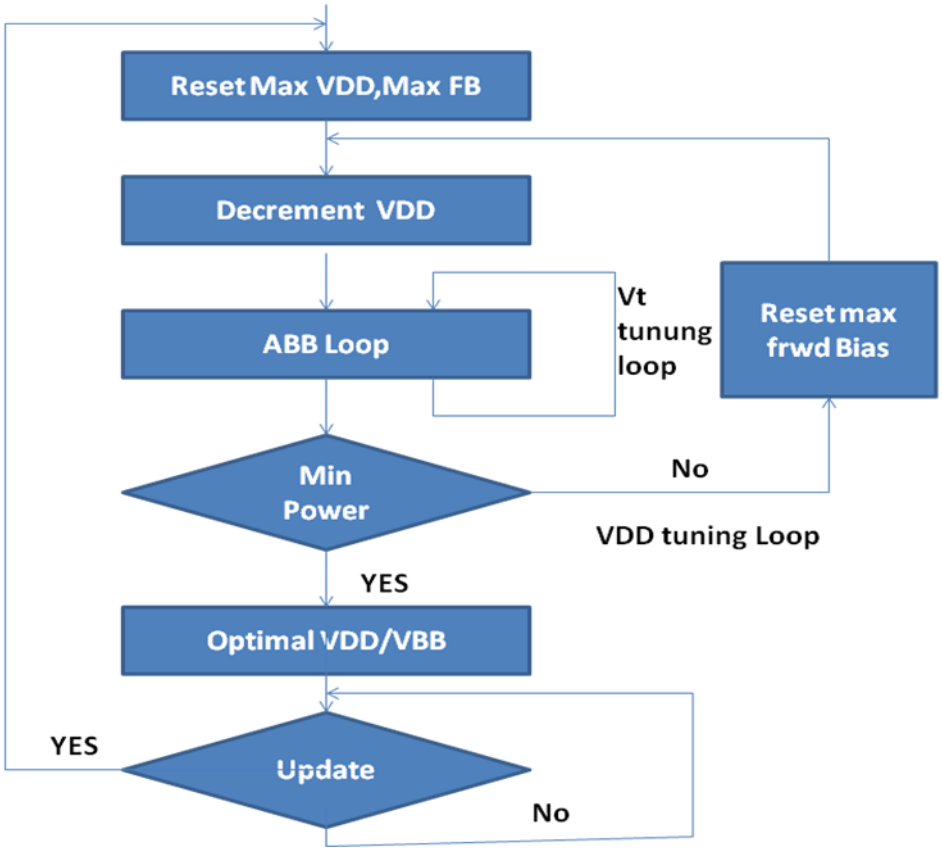

Fig. 3.2 Flowchart for automatic V_{dd} /V_{th} optimization.

The loop can be reactivated whenever the workload changes, or periodically updated to reflect changes in temperature or operating conditions. Because the ASB loop does not have to be constantly running, the overhead power utilization, which is already amortized across the whole chip, can be reduced even further. This ASB control loop is completely self-contained and should lock to the true minimum power configuration taking into account all possible current paths.

This minimum will result in the physically lowest power consumption achievable by tweaking both and subject to the constraint that the chips satisfy a target frequency. Even for technologies where the theoretical limit is not yet achievable using body biasing techniques or in cases where excessive forward bias at low degrades performance, it is still possible to use this structural design to find the minimum physical power condition.

The threshold voltage can be controlled by changing the body bias of the transistors and is called the adaptive body bias (ABB) method. For speed silicon, reverse body bias is applied to increase threshold and decrease leakage, whereas for slow silicon, forward body bias is applied to reduce threshold and improve performance. Here the body bias adjustment is done sparingly as needed based on the chip's process state, and is not a continuous changeable like the supply voltage.

However the point of minimum power depends on the ratio of Active to leakage power, with the former modulated by the movement issue. For media applications, the activity factor can vary a lot across different applications and hence, the most favorable settings for threshold and supply also diverge .Analogous to table based AVS, a table based AVTS scheme has been proposed where for different activity factors, the equivalent supply and body bias values are stored in the look up table. The activity factors are estimated for different applications off-line. During run-time, based on the application being run, the suitable activity factor is used to consult the look up table to obtain the settings for supply and body bias, which will minimize power. Adaptive voltage and threshold scaling aims to arrive at the optimal voltage and threshold values at run time, by not only adapting to the process and temperature like in AVS, but also to the dynamically varying activity conditions.

4.1 ADVANTAGES OF AVTS OVER AVS:

No voltage level converters

AVS or multiple VDD systems require a voltage level shifter whenever a low VDD signal is driving a high VDD receiver. Although the conventional level converters prevent the static power consumption, the Active power consumption is large enough to cancel out the power savings gained from supply voltage scaling. Since AVTS systems use the same supply voltage throughout the chip, no voltage level converters are required.

Simple hardware

Charge pumps are a simple solution for boosting voltages. No external inductors are needed and power consumption is very low compared to buck converters, which are used for AVS systems. Charge pumps are used for our AVTS system to generate the body bias voltages

Less power loss charging/discharging internal nodes

Transition energy wasted charging/discharging the VDD ground capacitance is the power overhead of the AVS scheme. For low-to-high and high-to-low transition of supply voltage, current is extracted or placed back to the power supply. Even though there is no computation during this cycle, transition energy is consumed. Since the supply voltage is fixed for AVTS, it has less transition energy loss while charging and discharging the internal nodes.

Improvement in noise immunity

Signal integrity has become an important issue for deep sub micron devices as crosstalk noise becomes considerable. Increasing VTH for low workload periods in AVTS will help improve noise immunity, especially for noise-susceptible circuits such as domino logic and pulsed flip-flops.

4.2 RESULTS AND DISCUSSION

To mitigate the Active leakage problem, a Active Vth Scaling (AVTS) scheme is presented. AVTS algorithm that can be studied and implemented for the design of VDD controller. VDD will be scaled and controlled according to the limits for the circuit. Power reduction technique can be applied to basic CMOS circuits and the results for average power are analyzed. Ex.Inveter, NAND, NOR. This idea can be extended to larger circuits in future.

4.2.1 VDD &VBS CONTROLLER:

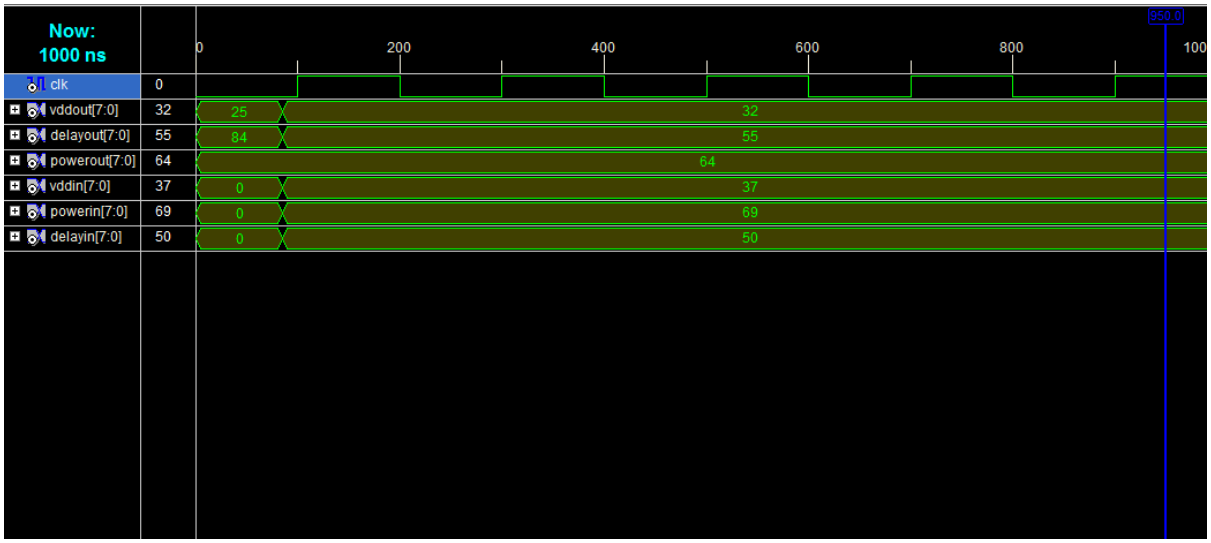

Fig 4.1 VDD controller Graph results

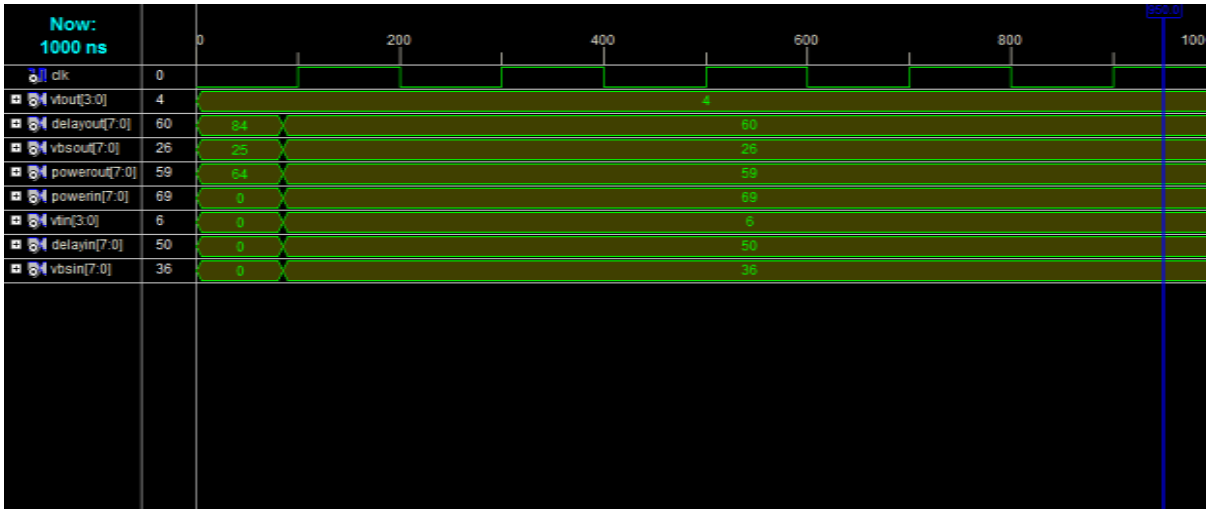

Fig 4.2 VBS controller Graph results

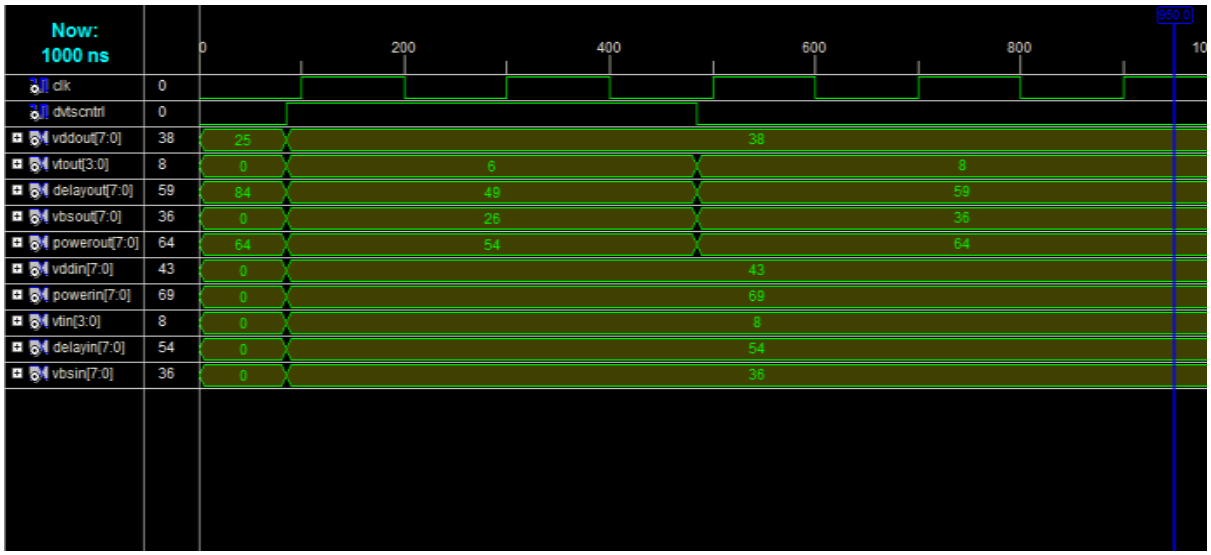

Fig 4.3 AVTS controller Graph results

III. CONCLUSION

An AVTS algorithm that can locate with varying activity is studied under simulation framework and validated with a test chip. Timing overhead of AVTS system and size of load circuit is analyzed as they limit the application of AVTS. The tracking performance of the algorithm can be improved by reducing the timing overhead. It can be inferred that for technology node with larger leakage currents, AVTS is more beneficial over AVS

IV. Acknowledgements

We would like to thank our parents and esteemed Bharath University Research and Development Chennai and our team members.

AUTHER'S PROFILE

S.Hari Prasath Sharma was born on 02/06/1989. He has obtained B.E. (ECE) Degree from Anna University Chennai, Tamil Nadu in the year 2010, who is currently pursuing Final year M.Tech. VLSI from Bharat University, Chennai, Tamil Nadu, India.

G.Vishnu Sankar was born on 10/09/1988. He has obtained B.E. (ECE) Degree from Anna University Chennai, Tamil Nadu in the year 2012, who is currently pursuing final year M.Tech. Embedded Systems from Bharath University, Chennai, Tamil Nadu, India.

S.M.K.Srikanth was born on 09/12/1990. He has obtained B.E. (ECE) Degree from Anna University Chennai, Tamil Nadu in the year 2012, who is currently pursuing final year M.Tech. Embedded Systems from Bharath University, Chennai, Tamil Nadu, India.

Dharitri Ray was born on 19/06/1989. She has obtained B.Tech. (ECE) Degree from Annamalai University Chidambaram, Tamil Nadu, who is currently pursuing Final year M.Tech. VLSI from Bharath University, Chennai, Tamil Nadu, India

REFERENCES

[1] J. Kao, M. Miyazaki, and A. Chandrakasan, "A 175-MV multiply-accumulate unit using an adaptive supply voltage and body bias architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1545–1554, Nov. 2002,

[2] K. Nose and T. Sakurai, "Optimization of VDD and VTH for low power and high speed applications," in *Proc. Asia South Pacific Des. Autom. Conf.*, 2000, pp. 469–474.

[3] M. Elgebaly and M. Sachdev, "Variation-aware adaptive voltage scaling system," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 5, pp. 560–571, May 2007.

[4] R. McGowan, C. Poirier, C. Bostak, J. Ignowski, M. Millican, W. Parks, and S. Naffziger, "Power and temperature control on a 90-nm Itanium family processor," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 229–237, Jan. 2006.

[5] T. Burd, T. Pering, A. Stratakos, and R. Brodersen, "A ACTIVEvoltage scaled microprocessor system," *IEEE J. Solid-State Circuits*,vol.35, no. 11, pp. 1571–1580, Nov. 2000.

[6] T. Kuroda, K. Suzuki, S. Mita, T. Fujita, F. Yamane, F. Sano, A. Chiba, Y. Watanabe, K. Matsuda, T. Maeda, T. Sakurai, and T. Furuyama, "Variable supply-voltage scheme for low-power high-speed CMOS digital design," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 454–462, Mar. 1998.

[7] Y. Ramadass and A. Chandrakasan, "Minimum energy tracking loop with embedded DC-DC converter enabling ultra-low-voltage operating down to 250 mV in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 256–265, Jan. 2008.