

Adaptive VLSI Framework for Image Reducing Algorithms

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Abstract

JPEG is one of the most used image compression standard which uses discrete cosine transform (DCT) to transform the image from spatial to frequency domain. An image contains low visual information in its high frequencies for which heavy quantization can be done in order to reduce the size in the transformed representation. Real-time data processing requires high speed which makes dedicated hardware implementation most preferred choice. The hardware of a system is favored by its lowcost and low-power implementation. These two factors are also the most important requirements for the portable devices running on battery such as digital camera. Image transform requires very high computations and complete image compression system is realized through various intermediate steps between transform and final bit-streams. Intermediate stages require memory to store intermediate results. The cost and power of the design can be reduced both in efficient implementation of transforms and reduction/removal of intermediate stages by employing different techniques. Direct implementation algorithm of DCT has the advantage that it is free of transposition memory to store intermediate 1-D DCT. Although recursive algorithms have been a preferred method, these algorithms have low accuracy resulting in image quality degradation. A non-recursive equation for the direct computation of DCT coefficients have been proposed and implemented in both 0.18 μm ASIC library as well as FPGA. It can compute DCT coefficients in any order and all intermediate computations are free of fractions and hence very high image quality has been obtained in terms of PSNR. In addition, one multiplier and one register bit-width need to be changed for increasing the accuracy resulting in very low hardware overhead. The architecture implementation has been done to obtain zig-zag ordered DCT coefficients. The comparison results show that this implementation has less area in terms of gate counts and less power consumption than the existing DCT implementations. Using this architecture, the complete JPEG image compression system has been implemented which has Huffman coding module, one multiplier and one register as the only additional modules, one multiplier and one register as the only additional modules. The intermediate stages (DCT to Huffman encoding) are free of memory, hence efficient architecture is obtained.

Keywords: JPEG, DCT (Discrete cosine transforms), FPGA (Field Programmable Gate Arrays), Huffman encoding, quantization, transformation.

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I. INTRODUCTION

Image Compression is one of the emerging technique of Digital System for storing, retrieving of digital media applications. The main problem of Image Compression is requiring less space for storage and computation speed. In this paper we address this problem and develop a memory efficient high speed architecture which is implemented based on orthonormalized multi-stage Fast-DST processing unit to perform lifting operation. The proposed multi-stage transform unit performs the split, predict and the update operations by considering the odd samples which are neglected in other lifting transforms. This results in speeding up the process because of the simultaneous execution of both samples. The RTU and CTU are erected with the aid of delay elements and the lifting coefficient, which further tends to attain the optimized processing speed. To address the problem of high cost of memory, multi stage proposed DST unit are combined to build a parallel multi-stage architecture which can perform multistage parallel execution on input image at competitive hardware cost. Finally, the proposed method attains better results when they are compared with existing in terms of memory complexity, low power, and low latency. The image compression is an important factor that involves huge data storage, transmission and retrieval such as for multimedia, documents, video conferencing, and medical imaging [1]. It is seen that the objective of image compression technique is to reduce redundancy of the

image information in order to have the capacity to store or transmit information in an efficient frame. Thereby utilizing the designing technologies of VLSI system we can ready to expel the image redundancy and also compress the image. Due to the fast advance of VLSI design technologies, numerous processors in light of sound and image signal processing have been created recently. The Very-Large Scale Integration (VLSI) is the process of creating incorporated circuits by combining a huge number of transistor-based circuits into a semiconductor chip. The principal of semiconductor chips held one included an ever increasing number of transistors, and as a consequence, more individual functions or systems were coordinated after some time. The principal incorporated circuits held just a couple of devices, maybe upwards of ten diodes, transistors, resistors, and capacitors, making it conceivable to fabricate at least one logic gates on a solitary device. Presently referred to reflective as Bsmall-scale integration[^] (SSI), enhancements in technique prompted devices with many logic gates, known as large scale integration (LSI), i.e. systems with no less than a thousand logic gates. The technology in the past presents the microprocessors which have a huge number of gates and individual transistors. The advancements in VLSI technology give capable devices to the acknowledgment of complicated image and video processing systems with the knowledge of lifting scheme. Prior the VLSI system utilized lifting based DWT (Discrete Wavelet Transform) for image compression. The execution of DWT in a practical system has issues. To begin with, the complexity of the wavelet change is a few times higher. Second, DWT needs additional memory for storing the intermediate computational results. In addition, DWT needs to process monstrous measures of information at high speeds. The utilization of software usage of DWT image compression gives adaptability to control, however it may not meet planning constraints in certain applications. Hardware execution of DWT has practical obstacles. To start with, that is the high cost of hardware execution of multipliers. Channel bank execution of DWT contains two FIR channels. It has customarily been actualized by convolution or the limited drive reaction (FIR) channel bank structures. Such usage requires both substantial numbers of arithmetic computations and storage, which are not attractive for either high speed or low power image/video processing applications . Nowadays the multiple problems have been achieved by using Memory-Efficient Architecture of 2-D Dual-Mode Discrete Wavelet Transform Using Lifting Scheme for Motion-JPEG2000. S-transform is performed by isolating the low-frequency information from high-frequency counterparts to expel the disadvantages of DWT. This operation can be acknowledged in various ways, which could be level-by-level, block-based or linear based transformation Compared with other previous architectures, the internal memory size of this architecture is very small. It adopts parallel reduce the internal and increase the operation speed. Shifters and adders are used to replace multipliers in the computation to reduce the hardware cost and low complexity in the VLSI implementation. Due to the characteristics of low memory size and high operation speed, it is suitable for VLSI implementation and can support various real-time image/video applications such as JPEG2000, motion-JPEG2000, MPEG-4 still texture object decoding, and wavelet-based scalable video coding Explosive development in the digital VLSI field, particularly in deep submicron CMOS Nano electronics, is powered by novel inventions in physics at the device level with technological progressions. In parallel to technological progressions, the performance of the system is quickly enhancing at the algorithms level by enlightened architectural designs, which progressively take into non-typical mathematical methods and optimization techniques that are precisely tailored for digital VLSI devices with superior performance.

1.1 Compressed sensing (CS) theory asserts that one can recover certain signals and images from far fewer samples than Nyquist rate [1]. However, the reconstruction of the signal from the CS measurements remains computationally intensive. The problem of signal recovery from CS measurements has remained very well studied in recent years and a fairly large number of algorithms have been proposed to reconstruct the signals from the CS measurements. In compressed sensing, a signal \mathbf{x} is reconstructed from a small set of linear random projections \mathbf{y} by solving the following optimization [2].

1.2 VLSI architecture An efficient VLSI architecture for minimized sorting network (Vasanth sorting) in rank ordering application to remove salt and pepper noise is proposed. The basic operation in salt and pepper noise removal is rank ordering. In this work, a novel 2D sorting technique referred to as Vasanth sorting is proposed for a fixed 3×3 window. Vasanth sorting requires only 25 comparators to sort 9 elements of the window. A parallel architecture is developed for Vasanth sorting with 25 comparators. The processing element of the parallel architecture is an 8-bit data comparator (Two cell comparator). The performance of the proposed sorting technique is compared with the different sorting technique which is targeted for XCV100-5bg560 on XILINX 7.1i and xc7v200-2flg1925 Xilinx 14.7 project manager respectively with Modelsim 10.4a for simulation and XST compiler tool for synthesis using VHDL.

II. METHODOLOGY

2.1 Introduction A digital image is two-dimensional functional in space where amplitudes at each location are called pixels. There are different types of images depending upon the different number of data bits per pixel for their representation. Quality of an image can be assessed either visually or by mathematical formulation. The

former is called subjective quality assessment and the later objective quality assessment. A common objective quality assessment metric for images obtained after decompression is PSNR (peak signal-to-noise ratio). Transform based lossy image compression is flexible as it can compress images at different qualities depending upon the application of the image. JPEG uses 8x8 block-wise 2-D DCT as the transform. DCT has very high energy compaction and its performance is almost similar to optimal Karhunen-Lo'ev transform (KLT) with the advantage of constant kernel and less computational complexity. Still, for the hardware implementation, similar kind of transform which will have less computational complexity and hence less hardware requirement with performance almost similar to DCT can be a preferred choice.

2.2 Discrete Cosine Transform (DCT) DCT is an orthogonal transform. Karhunen-Lo'ev transform (KLT) is optimal in class of orthogonal transforms like Fourier transform, Walsh-Hadamard transform and Haar transform and has the best energy compaction [72, 79]. However, KLT is not ideal for practical image compression as its basis vectors has to be calculated according to the pixel values of the image (i.e., KLT is a data dependent). For each image, there will be separate basis vectors that also need to be included in the compressed image for the decompression process. It was found that DCT performs close to KLT and their performances are also close with respect to rate-distortion criterion (quality at different compression) [79]. In addition, there are several fast and hardware efficient algorithms available for the computation of DCT [80–87]. Therefore, DCT became the widely used transform for lossy image encoding/compression and also in the several other signal processing applications.

2-D DCT Equation

For a NxN 2-D data X(i, j), 0 ≤ i ≤ N-1 and 0 ≤ j ≤ N-1, NxN 2-D DCT is given by [64]

$$F(u, v) = \frac{2}{N} C(u)C(v) \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} X(i, j) \times \cos\left(\frac{(2i+1)u\pi}{2N}\right) \cos\left(\frac{(2j+1)v\pi}{2N}\right)$$

where, 0 ≤ u ≤ N-1 and 0 ≤ v ≤ N-1 and C(u), C(v) = 1/2 for u, v=0, C(u), C(v) = 1 otherwise. The 2-D DCT equation is separable transform and can be evaluated by first taking the 1-D DCT to rows followed by 1-D DCT to columns, where 1-D DCT is given by,

$$F(u) = \sqrt{\frac{2}{N}} C(u) \sum_{i=0}^{N-1} X(i) \cos\left(\frac{(2i+1)u\pi}{2N}\right)$$

With, C(u) defined as above. Fig.2.1 shows the 2-D DCT calculation from 1-D DCT using separable property. DCT transforms the spatial data into frequency domain.

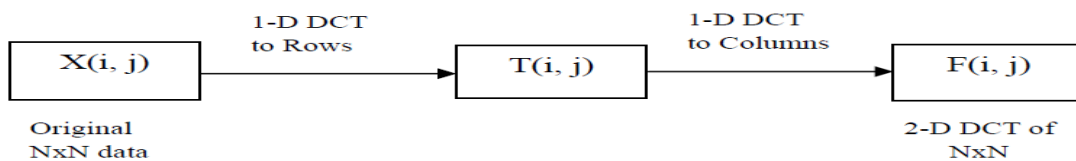


Fig. 2.1 2-D DCT from separable property

2.3 Image Reconstruction by selective DCT coefficients

DC coefficient of DCT contains the average pixel values of the image. This is true for the block based transform as well. In case of block based transform, DC coefficients of each block carry most of the signal energy of that block and therefore, DC coefficients of the image have highest energy as compared to the average energy possess by total AC coefficients of entire blocks. This is shown in Fig.3.7, where Lena and Peppers images are first DCT transformed in 8x8 blocks. Then, AC coefficients of each block are discarded (quantized to zero) and image is reconstructed by Inverse DCT (IDCT) with the help of only DC coefficients of each block. Energy compaction property of DCT.

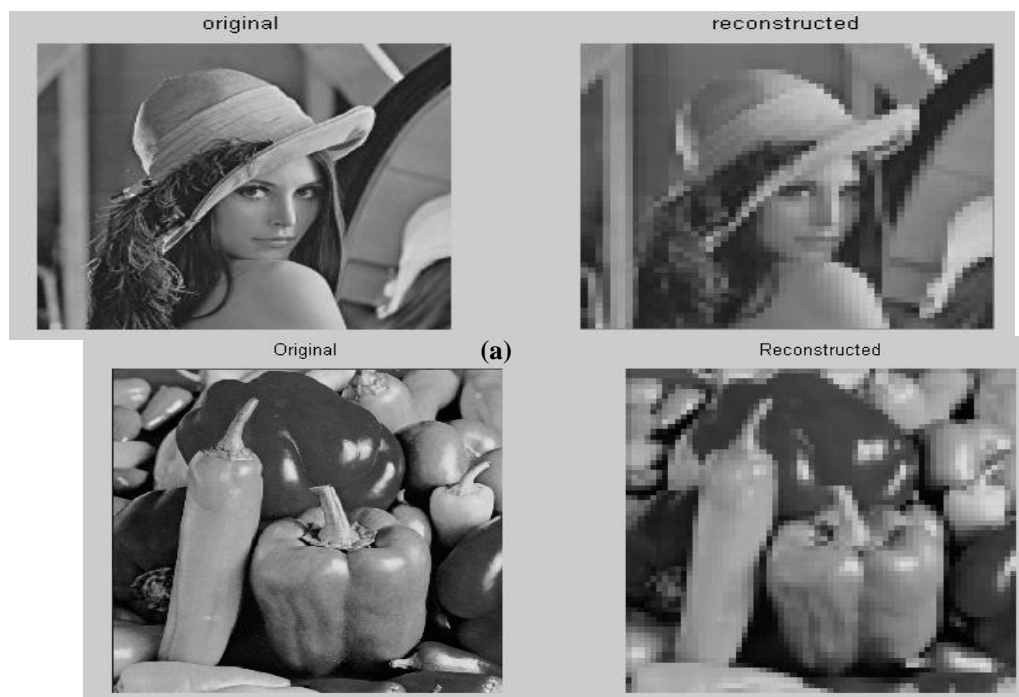


Fig. 2.2 Original (left) and reconstructed (right) image after quantizing all AC coefficients of 8x8 DCT to zero (a) Lena and (b) Peppers

III. RESULT AND DISCUSSION

The results obtained are as discussed below

Coefficients discussion clarify that most of the image energy is contained in few low order DCT coefficients. This observation can be exploited to reduce the computation of DCT in both hardware and software implementations. Four types of images are JPEG compressed and decompressed in three cases by selectively taking 8x8 DCT coefficients.

Case 1: All 64 DCT coefficients are taken for reconstruction.

Case 2: Only first row and first column DCT coefficients are taken for reconstruction.

Case 3: Only first 15 DCT coefficients in zig-zag ordered are taken for reconstruction.

TABLE 4.1 shows the percentage improvement in compression ratio (CR) in case 2 and case 3 with respect to case 1. Shadow rows shows the CR for heavy quantization (higher value of quantization parameter i.e., “quality”). Fig.3.1 shows the reconstructed images in above mentioned three cases. Reconstructed images are shown for the quality comparison as psychovisual information (not visible to eyes [88]) is removed by discarding the high frequency coefficients. The following observations can be made from TABLE 3.1 and Fig. 3.1. There is much improvement in compression ratio in case of low quantization without visual image quality degradation. At the higher quantization, smooth image (like Peppers, Lena) shows little improvement in compression ratio while detailed images (Cameraman) show still high improvement without visual quality degradation when first 15 low frequency coefficients are taken for image reconstruction, quantizing rest to zero. From these observations, it can be concluded that DCT algorithm, which computes DCT coefficients one by one sequentially, can be made computationally efficient (at the same time low energy consuming) and faster by selectively taking the DCT coefficients for the image quality requirements. In addition, higher compression can be achieved by doing so.

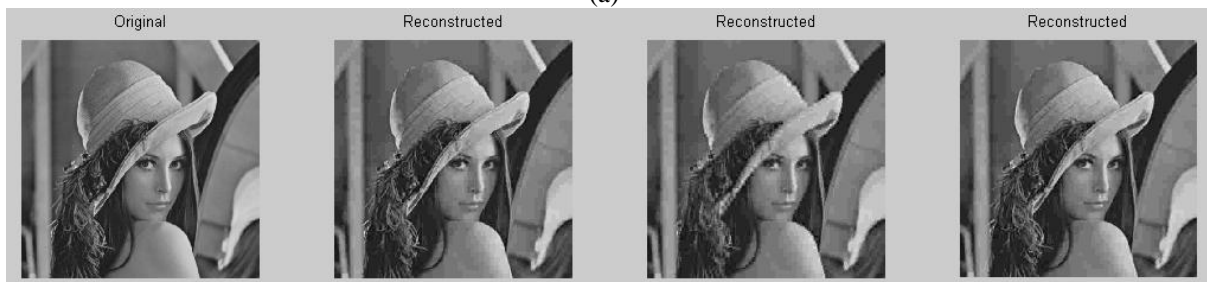
TABLE 3.1 Compression Ratios Obtained For Different Quantization Level

Image	Quality	Compression ratio in case 1 (all 64 DCT coefficients taken)	Compression ratio in case 2 (first row and first column DCT coefficients taken)	Compression ratio in case 3 (first 15 coefficients taken)	% improvement in compression ratio in case 2 (as compared to case 1)	% improvement in compression ratio in case 3 (as compared to case 1)
Lena (448x448)	Quality=1	12.66	19.08	14.16	50.7%	11.84%
	Quality=5	33.74	39.96	34.09	18.4%	1.0%
Peppers	Quality=1	12.50	18.17	14.02	45.3%	12.1%

(512x512)	Quality=8	41.50	45.24	41.58	9.0%	0.1%
Crowd (512x512)	Quality=1	6.88	11.61	7.96	68.7%	154.7%
	Quality=5	17.48	23.87	17.62	36.5	0.8%
Cameraman (256x256)	Quality=1	9.64	16.58	14.30	73%	38%
	Quality=3	19.42	27.98	22.06	44%	14%



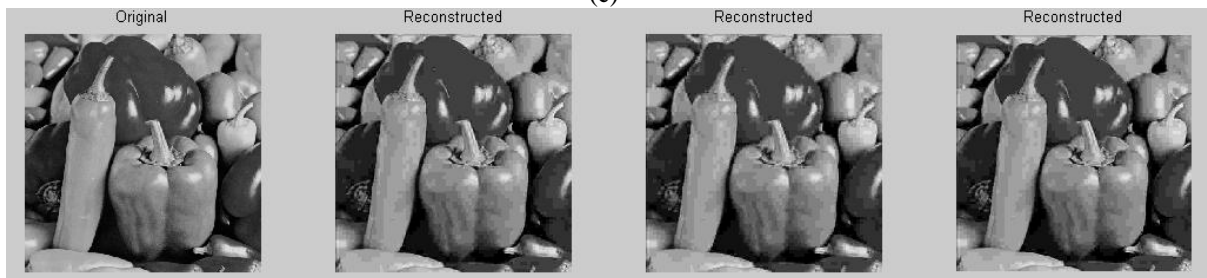
(a)



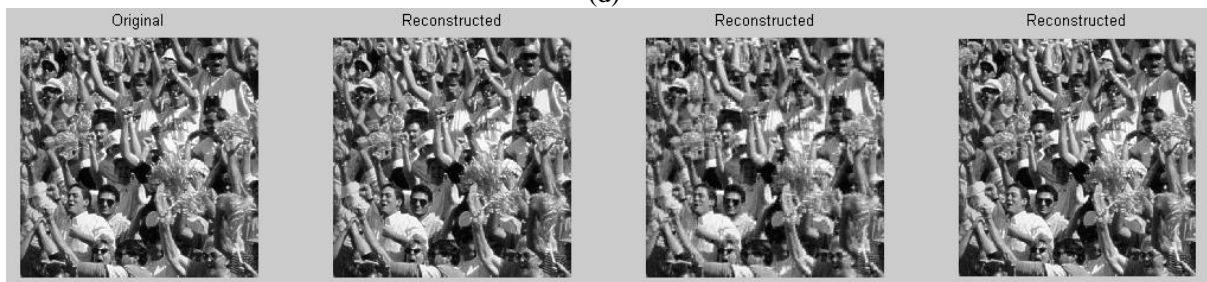
(b)



(c)



(d)



(e)

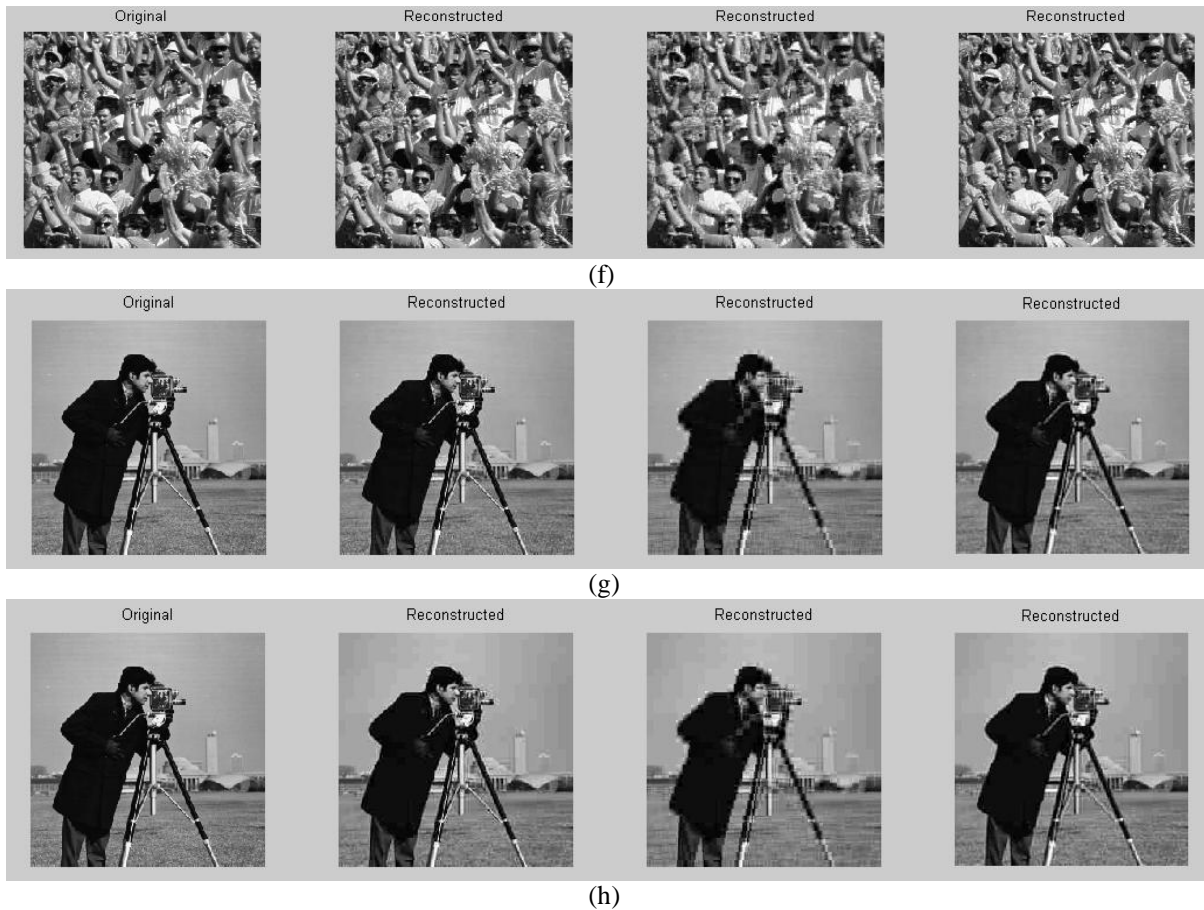


Fig 3.1 From left to right, original image, reconstructed image by taking all DCT coefficients, reconstructed image by taking first row and first column DCT coefficients, reconstructed image by taking first 15 coefficients in zig-zag order of (a) 448x448 Lena, quality=1, (b) 448x448 Lena, quality=5, (c) 512x512 Peppers, quality=1, (d) 512x512 Peppers, quality=8(e) 512x512 Crowd, quality=1, (f) 512x512 Crowd, quality=5, (g) 256x256 Cameraman, quality=1, (h) 256x256, Cameraman, quality=3.

IV. CONCLUSION

Digital image representation and its quality measurement metric have been described in this work. The energy compaction property of DCT has been studied by decompression the standard image with selected low frequency DCT coefficients. High compression can be obtained when image are compressed with few lower DCT coefficient without visual distortion. From simulation, it is found that it performs better than DCT in high compression.

REFERENCES

- [1] G kiranmaye & Srinivasulu Tadisetty “ A novel ortho normalized multi stages fast stockwell transform based memory aware high speed VLSI implementation for image compression” Springer Science and Business Media, LLC, part of Springer Nature 2019; 10 jan 2019.
- [2] Kota Naga Srinivasarao Batta , Member, IEEE, and Indrajit Chakrabarti, Member, IEEE “VLSI Architecture for Enhanced Approximate message passing Algorithm. IEEE Transactions On Circuits And Systems For Video Technology, Vol. 30, No. 9, September 2020
- [3] K. Vasanth a, E. Sindhu b, R. Varatharajan c, “VLSI architecture for Vasanth sorting to denoise image with minimum comparators” Elsevier Science Direct; 2019.
- [4] R. C. Gonzalez, R. E. Woods, Digital Image Processing, 2nd.Ed. Prentice Hall, 2002.
- [5] Chin-Hwa Kuo, Tzu-Chuan Chou and Tay-Shen Wang, “An efficient spatial prediction-based image compression scheme,” IEEE Transactions on Circuits and Systems for Video Technology, vol.12(10), pp. 850- 856, Oct. 2002.
- [6] Chen Shoushun, Amine Bermak, Wang Yan and Dominique Martinez, “Adaptive-Quantization Digital Image Sensor for Low-Power Image Compression,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol.54(1), pp.13-25, Jan. 2007.
- [7] M.D. Reavy, C.G.Boncellet, “An algorithm for compression of bilevel images,” IEEE Transactions on Image Processing, vol.10(5), pp.669-676, May 2001.
- [8] Debin Zhao, Wen Gao, and Y. K. Chan, “Morphological representation of DCT coefficients for image compression,” IEEE Transactions on Circuits and Systems for Video Technology, vol.12(9), pp. 819-823, Sep. 2002.

- [9] K. A. Kotteri, A. E. Bell and J. E. Carletta, "Multiplierless filter Bank design: structures that improve both hardware and image compression performance," IEEE Transactions on Circuits and Systems for Video Technology, vol.16(6), pp. 776- 780, June 2006.
- [10] N. N. Ponomarenko, K. O.Egiazarian, V. V.Lukin, and J. T. Astola, "High-Quality DCT-Based Image Compression Using Partition Schemes," IEEE Signal Processing Letters, vol.14(2), pp.105-108, Feb. 2007.
- [11] Xinpeng Zhan, "Lossy Compression and Iterative Reconstruction for Encrypted Image," IEEE Transactions on Information Forensics and Security, vol.6(1), Mar. 2011.
- [12] Yi-Huang Han and Jin-Jang Leou, "Detection and correction of transmission errors in JPEG images," IEEE Transactions on Circuits and Systems for Video Technology, vol.8(2), pp.221-231, Apr. 1998.
- [13] R.Chandramouli, N.Ranganathan and S.J. Ramadoss, "Adaptive quantization and fast error-resilient entropy coding for image transmission," IEEE Transactions on Circuits and Systems for Video Technology, vol.8(4), pp.411-421, Aug. 1998.
- [14] V. DeBrunner, L. DeBrunner, Wang Longji and S. Radhakrishnan, "Error control and concealment for image transmission," IEEE Communications Surveys & Tutorials, vol.3(1), pp.2-9, First Quarter 2000.
- [15] P.P. Dang and P.M. Chau, "Robust image transmission over CDMA channels," IEEE Transactions on Consumer Electronics, vol.46(3), pp.664-672, Aug 2000.