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A Comparative Study of Power Inverter Topology and Control Structures for Renewable Energy Recourses

Dr. Khirod Kumar Rout, Sandip Kar Mazumdar, Sagarika Patro,Poonam Tripathy

Department of Electrical and Electronics Engineering, NM Institute of Engineering and Technology,Bhubaneswar , Odisha
Department of Electrical and Electronics Engineering, Raajdhani Engineering College,Bhubaneswar,Odisha
Department of Electrical and Electronics Engineering,Aryan Institute of Engineering and Technology Bhubnaeswar , Odisha
Department of Electrical and Electronics Engineering,Capital Engineering College,Bhubaneswar,Odisha

Abstract*: Voltage boosting is very essential issue in renewable-energy fed applications. The classical two-stage power conversion process is typically used to interface the renewable energy sources to the grid. For better efficiency, single- stage inverters are recommended In this paper we make MATLAB-Simulink models of the three types of multilevel inverters: Cascaded type, Diode clamped and Capacitor clamped. A relative study of the carrier frequency modulation techniques is also presented on the basis of THD under various modulating indices. Graphs have been plotted based on these results.*
Index Terms: *Pulse width modulation converters, Multilevel Inverters, Total Harmonic Distortion*

I. NOMENCLATURE

PD: Phase Disposition
APD: Alternative Phase Disposition POD: Phase Opposition Disposition THD: Total Harmonic Disposition SDCS: Single Direct Current Source

II. INTRODUCTION

Theoretical and mathematical models of multilevel inverters can be found in numerous papers [1 - 4].This paper tries to develop the Simulink model of these inverters and to make a comparative study of the carrier based modulation strategies. The results are obtained by comparing the T.H.D. of the different voltage waveforms.

III. DIODE CLAMPED MULTILEVEL INVERTER

The figure 1 shows a 5 level diode clamped multilevel inverter. The number of levels of a diode clamped inverter, if N is the total no of capacitors used is N + 1.Increasing the levels in an inverter leads to reduced harmonics in the output voltage. So figure 1 is a 5 level inverter.It is to be noted that an m-level diode-clamped inverter has an m- level output phase voltage and a (2m-1)-level output line voltage [1]. i.e above inverter has 5 level phase voltage waveform and 11 level line voltage waveform .Also although each switch has to block a voltage of V

,different diodes will have to block different voltages. For example D2 will have to block 2 Vdc. So different diodes should have different ratings. For diodes having same ratings, any m level inverter will have to employ (m – 1)*(m – 2) diodes .Thus, the number of blocking diodes is quadratically related to the number of levels in a diode- clamped converter. The main advantages and disadvantages of diode clamped inverters are given below:

Advantages:

- All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter.

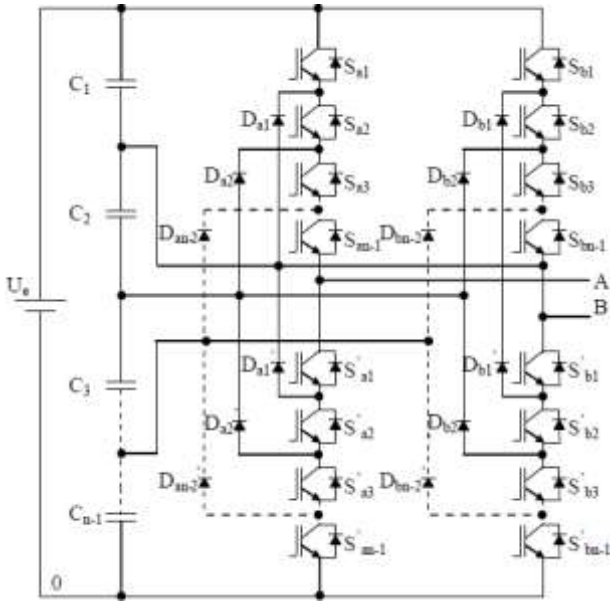

Fig. 1. 5 level diode clamped multilevel inverter

For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.

- The capacitors can be pre-charged as a group.
- Efficiency is high for fundamental frequency switching.

Disadvantages:

- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

IV. FLYING CAPACITOR MULTILEVEL INVERTER

The circuit topology of the flying capacitor multilevel inverter is shown in Figure 2. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.

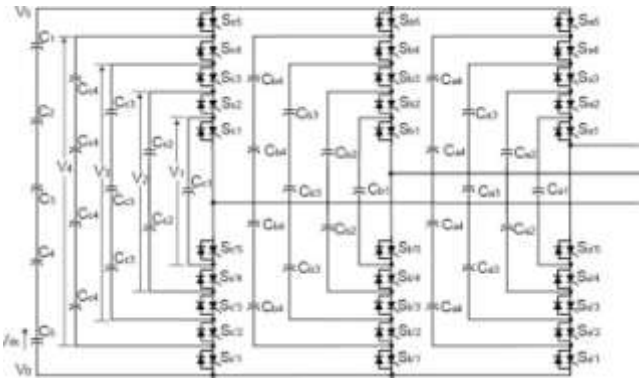

Fig. 2. flying capacitor multilevel inverter

The switching pattern of flying capacitor inverter is same as that of diode clamped inverter[1], however there are phase redundancies in former, which give a scope of better control for charging and discharging of capacitors. Following table shows the redundancies for obtaining different voltage levels.

Voltage V_{ao}	Switch State									
	S_{21}	S_{24}	S_{23}	S_{22}	S_{11}	S_{14}	S_{13}	S_{12}	S_{01}	S_{04}
	$V_{ao} = 5V_{dc}$ (no redundancies)									
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
	$V_{ao} = 4V_{dc}$ (4 redundancies)									
$5V_{dc} - V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc} - 3V_{dc} + 2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc} - 2V_{dc} + V_{dc}$	1	1	1	0	1	0	0	0	1	0
	$V_{ao} = 3V_{dc}$ (3 redundancies)									
$5V_{dc} - 2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc} - V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc} - V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc} - 3V_{dc} + V_{dc}$	1	1	0	0	1	0	0	1	1	0
$4V_{dc} - 2V_{dc} + V_{dc}$	0	1	1	0	1	1	0	0	1	0
	$V_{ao} = 2V_{dc}$ (6 redundancies)									
$5V_{dc} - 3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc} - 4V_{dc} + V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc} - 2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc} - 4V_{dc} + V_{dc}$	0	1	0	0	1	1	0	1	1	0
$4V_{dc} - V_{dc}$	0	0	1	1	0	1	1	0	0	1
$4V_{dc} - 2V_{dc} + V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
	$V_{ao} = V_{dc}$ (4 redundancies)									
$5V_{dc} - 4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc} - 3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc} - 2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc} - V_{dc}$	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
	$V_{ao} = 0$ (no redundancies)									
0	0	0	0	0	0	1	1	1	1	1

Table 1. Redundancies for obtaining different voltage levels.

V. CASCADED MULTILEVEL INVERTERS

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 3. Each separate dc source is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4. To obtain +Vdc, switches S1 and S4 are turned on, whereas –Vdc can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources.

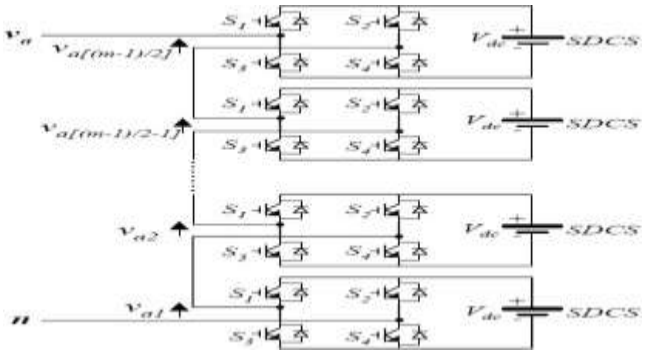

Fig. 3. Cascaded Inverter

The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows [1].

Advantages:

- The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages:

- Separate dc sources are required for each of the H- bridges. This will limit its application to products that already have multiple SDCSs readily available.

VI. MODULATION TECHNIQUES

Various modulating schemes have been discussed in multilevel inverters in literature [1,2,4].Some of them are discussed below. It is to be noted that the modulation can be achieved in the case of multilevel inverters in two ways:

1) By altering the modulating frequency
2) By altering the carrier frequency.

VI .1 Sinusoidal PWM:

For an m-level inverter, m-1 carriers with the same frequency fc and the same amplitude Ac are disposed such that the bands they occupy are contiguous. The reference waveform has peak-to-peak amplitude A m, a frequency fm, and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier

is switchedoff[1].

$$m_f = \frac{f_c}{f_m}$$

Below figure shows SPWM modulation scheme for ma = .8 and mf = 21.

$$m_a = \frac{A_m}{(m-1)\cdot A_c}$$

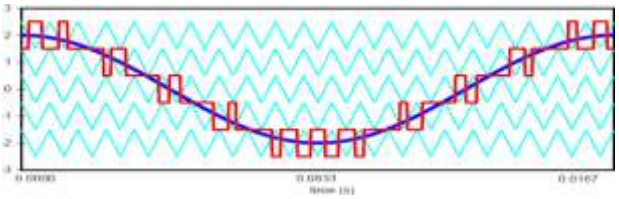

Fig. 4. Sinusoidal PWM

VI. 2 THPWM:

In this scheme, a third harmonic wave having same frequency as that of prime modulating wave and having a magnitude of about 25% is added to the prime wave. This increases the output voltage and the THD of the resultant wav is also increased. However, the switching losses in the top most level are decreased in this scheme.

Carrier Based Modulation Scheme:

Here the carrier frequency bands are given a phase difference between each other [3]. Thus three types of modulation can be achieved:

VI.3. Alternative Phase Opposition Disposition (APOD) Where each carrier band is shifted by 180° from the adjacent bands.

VI.4 Phase Opposition Disposition (POD) – Where the carriers above the Zero reference are in phase, but shifted by 180° from those carriers below the zero reference.

VI.5 Phase Disposition (PD)- Where all the carriers are in phase with each other.

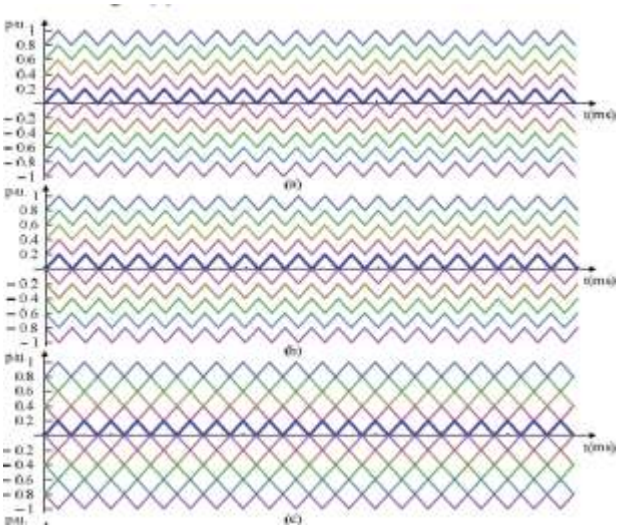

Fig.5. Multilevel carrier waveforms (a) PD, (b)POD, (c) APD

Advantages of multicarrier PWM techniques:

- Easily extensible to high number of levels.
- Easy to implement.
- To distribute the switching signals correctly in order to minimize the switching losses.
- To compensate unbalanced dc Sources.

VII. RESULTS

The carrier based modulation schemes were implemented on diode clamped , Flying capacitor and cascaded 5 level inverters. The following graphs are plotted against the modulation indices and the THD of the waveforms for the three types of inverters.

The modulating wave is a pure sinusoid , having f = 50 Hz. The carrier frequency is chosen to be 1000 hertz.

Table 2 and Fig.11 shows the variation of the THD with modulation index in case of a cascaded 5 level inverter.

Table 3 and Fig.12 shows the variation of the THD with modulation index in case of a Neutral point clamped 5 level inverter.

Table 4 and Fig. 13 show the variation of the THD with modulation index in case of a flying capacitor 5 level inverter.

The Red Line represents Alternative Phase Disposition, blue gives phase opposition disposition and green gives the phase disposition methods.

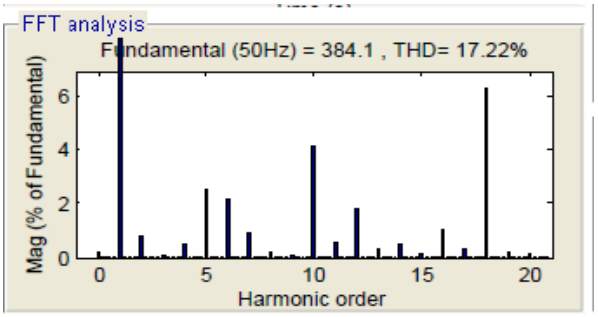

Fig. 6 Flying Capacitor ma= 1;mf = 20;PD

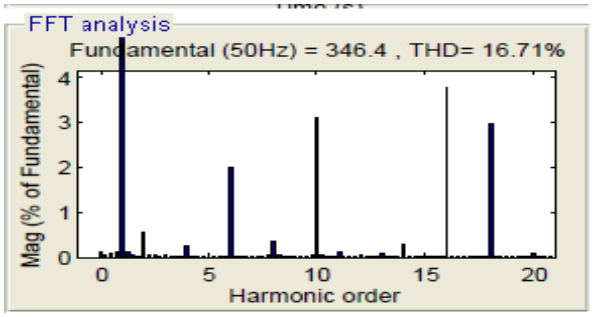

Fig. 7 Diode Clamped ma = 1;mf = 20;PD

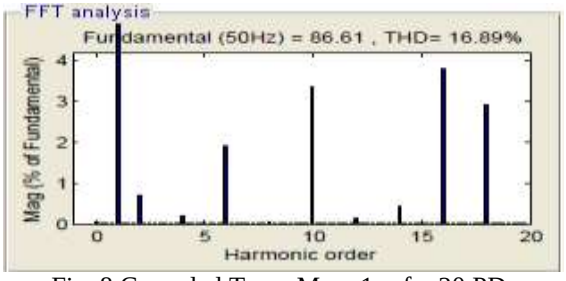

Fig. 8 Cascaded Type. Ma = 1;mf = 20;PD

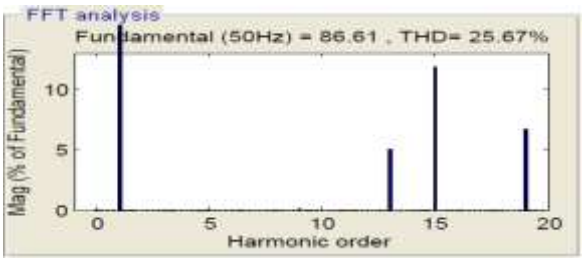

Fig. 9 Cascaded Type ma = 1;mf = 20;APD

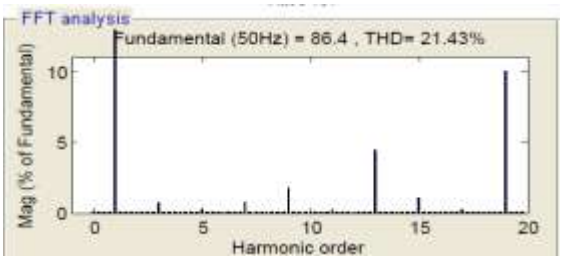

Fig. 10 Cascaded Type ma = 1;mf = 20;POD

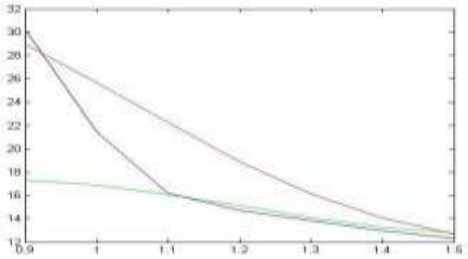

Fig 11 CASCADED 5 LEVELS

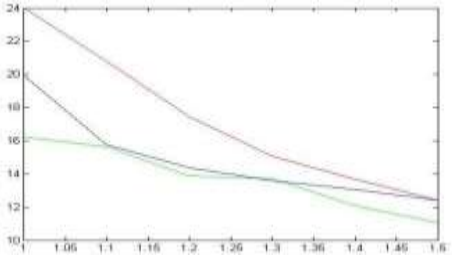

Fig 12 Neutral Point Clamped 5 level

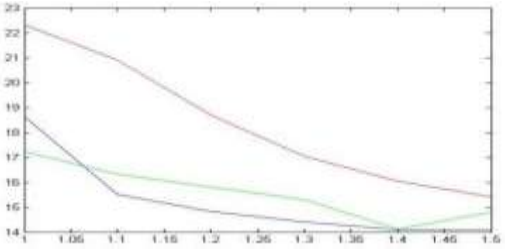

Fig 13 Flying Capacitor 5 level

m	Phase Disposition	Phase Opposition Disposition	Alternative Phase Disposition
1.5	12.79	12.32	12.70
1.4	13.26	12.97	14.07
1.3	14.05	13.84	16.14
1.2	15.10	14.72	18.88
1.1	16.07	16.17	22.28
1.0	16.89	21.43	25.67
.9	17.30	30.19	28.93

Table 2 Cascaded 5 level

M	Phase Disposition	Phase Opposition Disposition	Alternative Phase Disposition
1.5	11.03	12.40	12.41
1.4	12.06	13.03	13.66
1.3	13.69	13.59	15.07
1.2	13.85	14.36	15.07
1.1	15.63	15.77	20.77
1.0	16.20	19.92	25.65

Table 3 Neutral Point Clamped 5 Level

m	Phase Disposition	Phase Opposition Disposition	Alternative Phase Disposition
1.5	14.79	14.09	15.42
1.4	14.13	14.09	16.03
1.3	15.30	14.40	17.03
1.2	15.79	14.82	18.70
1.1	16.34	15.51	20.90
1.0	17.22	18.64	22.21

Table 4 Flying Capacitor 5 level

VIII. CONCLUSION

With the above observations, we can conclude that:-

This paper has dealt with a novel solution for single-phase grid-connected converters. The PWM strategy was chosen in order to obtain the minimum number of commutations to maximize efficiency

1) In case of the cascaded multilevel inverters, phase disposition method gives best results in terms of THD. Both Alternative Phase disposition method and Phase Opposition Disposition method are not suitable.

2) In the case of neutral point clamped inverters, the phase disposition is the best method for carrier wave, followed by phase opposition disposition .However alternative phase disposition method gives worse results.

3) In case of flying capacitor inverters, the phase opposition disposition method gives best results for high values of modulation index , however for low modulation index , phase disposition method is better .Alternative phase disposition method gives the worst results.

Also, from the FFT analysis shown in figure 6, 7, 8 ,9 , 10,

11 it is seen that in POD,APD schemes higher level harmonics are being generated, while in PD schemes, lower order harmonics are generated ,having very low magnitudes.

It can be clearly seen that the choice of carrier wave is also important so as to reduce the THD of the voltage waveform in a multilevel inverter.

In multilevel PWM, the switching frequency can be less than or greater than the

carrier frequency and is a function of the displacement phase angle between the carrier set and the modulation waveform .By adjusting the displacement phase angle in multilevel PWM switching strategies, switching losses can be minimized for a more efficient multilevel inverter[2].

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