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PID Compensator Control Scheme of Synchronous Buck DC-DC Converter with ZVS Logic Circuit

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Abstract *: This paper deals with PID compensator control of Synchronous Rectifier (SR) Buck Converter to improve its conversion efficiency under different load conditions with the help of a Zero Voltage Switching(ZVS)Logic Circuit. Since the freewheeling diode is replaced by a high frequency switch MOSFET in this buck configuration, the SR control technique itself will be sufficient under heavy load condition to attain better normal mode performance. However, this technique does not hold well in light load condition, due to increased switching losses. A newPID compensator control techniqueis introduced in the paper will enable synchronous buck converter to realize ZVS, while feeding light load. This is also cost effective and highly efficient simple control method without use of extra auxiliary switches and RLC components. This control technique also proved to be efficient under input voltage variations. Simulation is done for proving stabilization provided by the PID compensator with the help of ZVS logic circuit for synchronous rectifier (SR) buck converter in MATLAB Simulink.*

Keywords *-Discontinuous Conduction Mode (DCM), Proportional-Integral-Derivative (PID), Synchronous Rectifier (SR), Zero Current Detector (ZCD), Zero Voltage Switching (ZVS)*

I. Introduction

Over the years of development in the portable device industry, different requirements such as improved battery life, small size, low cost, high efficiency and easy control are to be satisfied for a better portable device. The day by day increasing energy demand from power systems has made power consumption as the first preference. To almost achieve these demands, engineers worked hard to develop efficient conversion techniques. High efficiency conversion of power supplies helps to decrease the battery-operated devices power consumption, and thereby increases the devices operating life and also achieves reduced battery drain. In addition, if a fairly large amount of power is dissipated by these power devices, they should be adequately cooled by mounting on heat sinks. Thus the heat can be transferred to the air in the surrounding atmosphere. Heat sinks and other cooling arrangements will make the whole system bulky and large. The need for heat sinks and relaxes thermal design considerations will be reduced by decreased power dissipation in the power supply. These added benefits will result in the popularity of switching regulators which have fairly high efficiency and small size [2].

In synchronous buck DC-DC converterconfiguration [3], the two MOSFETs used are synchronized and can be shown in figure 1. Synchronous Buck converter is similar to the conventionalbuck converterexcept the freewheeling diode is paralleled with SR switch Q2so that conduction loss is reduced.It is observed that the efficiency decreases when the load becomes heavy or light. As load becomes light especially where the load current is small, the efficiency drops to extremely low very quickly. Since the portable devices are operating in low-power standby mode for a majority of the time, which is in the light load condition, the poor load efficiency at this condition can ridiculously reduce the battery operating time. Thus light-load efficiency improvement is critical and important for portable devices. [4]

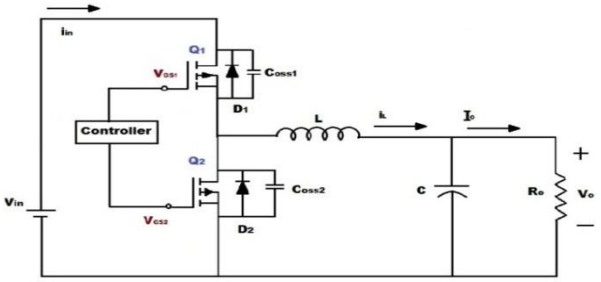

Figure 1. Synchronous Buck DC-DC Converter

Many techniques have been proposed to reduce the switching losses arising from switching frequency. Pulse width modulation (PWM)[5], Pulse frequency modulation (PFM) control [6] [7], [8] and double-mode control with pulse width modulation (PWM) and pulse frequency modulation (PFM) have been widely used [9]. According to the previous researches, the PWM-controlled converter has lower conversion efficiency than the PFM-controlled converter in light loads, whereas in heavy load condition, the PWM-controlled converter has got better conversion efficiency compared to PFM-controlled converter[10]-[13]. Therefore, some studies decided to combine the advantages of both the control methods to form a new control method called Dual mode control. In this technique, PFM is used in light load condition, whereas PWM is chosen in heavy load condition. This method can achieve better efficiency and also the nonlinear inductor is used for lowering switching frequency at light load condition [14]. However, large output voltage transients and sub harmonic noise occurs during transition between PWM and PFM. The switching frequency is also unpredictable and requires complicated fabrication materials because of the variable frequency operation. But other technique namely resonant gate drive uses an inductor and two diodes provided to clamp and recover drive energy (clamped gate voltage). Also the circuit timing is adjusted to cycle inductor current during driving transitions (fast driving speed) [15] - [17]. But the requirement of extra auxiliary switch and passive components and gate-source voltage over drive are its disadvantages. Several techniques like zero voltage switching (ZVS) [18] - [20] and digital control [21]-[23], have been used, but the application of these techniques are seem to be much complicated. ZVS and the digital control technique have better performance but need extra auxiliary switches and RLC passive components. Moreover, the controller used is a digital system processor which will result overall cost to be high.

The new control strategy with PID compensator and ZVS control logic in this paper enables an SR buck converter to have increased light load efficiency with ZVS technique without the requirement of extra auxiliary switches or RLC passive components. This control technique is of least cost and control method is also easy. Furthermore, the SR control strategy can be used to a dc low voltage outputs. The output voltage V (t) must be maintained within specified limits irrespective of the changes in the input line voltages and output loads. This is accomplished by using negative- feedback control system, where converter output V_O is compared with its reference value $V_{O,ref}$. The compensated error amplifier (PID compensator network) produces the control voltage which is used to adjust the duty cycle'd' of the switches in the converter. But in this converter type, no auxiliary circuit is present for reducing the switching losses. Thus this converter can be used only for low switching frequency applications.

II. Operating Stages

The operation of an SR buck converter grouped into eight stages based on the status of the two switches and load conditions. The oscillograph of the inductor current and control signals in the eight operating stages of an SR buck converter is shown in Figure 3. Based on different load conditions whether heavy load or light load and according to the methods introduced here, there are two kinds of operating stage combinations. The first operating stage combination is in the heavy load condition, i.e., Stage 1-Stage 2; whereas the second operating stage combination is in the light load condition, i.e., Stage 1-Stage 6.The following assumptions are made to simplify the analysis.

1. The output load voltage is assumed as constant voltage source due to large output capacitance.
2. No losses occur in any part of the circuit, i.e. all components in the circuit are assumed to be ideal.

2.1 Stage 1(t_0 -t_1):

In this state, the main switch Q1 is turned ON and the SR complementary switch Q2 is made to turn OFF. The path of conduction is shown in figure 2.

$$\boldsymbol{i_L(t) = i_L(t_0) + \frac{(V_{in}-V_O)}{L}(t - t_0)} \textbf{(1)}$$

The inductive current equation is given above is same as that of stage 1 of heavy load condition.

2.2 Stage 2(t_1- t_2):

At the instant of t_1, the SR complementary switch Q2 is switched ON and the main switch Q1 is made to turn OFF. The path of conduction is shown in figure 2 .The inductive current equation and the parasitic capacitive voltage equation is the same as that of stage 2 in heavy load condition and can be expressed as

$$\boldsymbol{i_L(t) = i_L(t_1) + \frac{(-V_O)}{L}(t - t_1)}\textbf{(2)}$$

$$\boldsymbol{v_{Coss1}(t) = V_{in}} \quad \textbf{(3)}$$

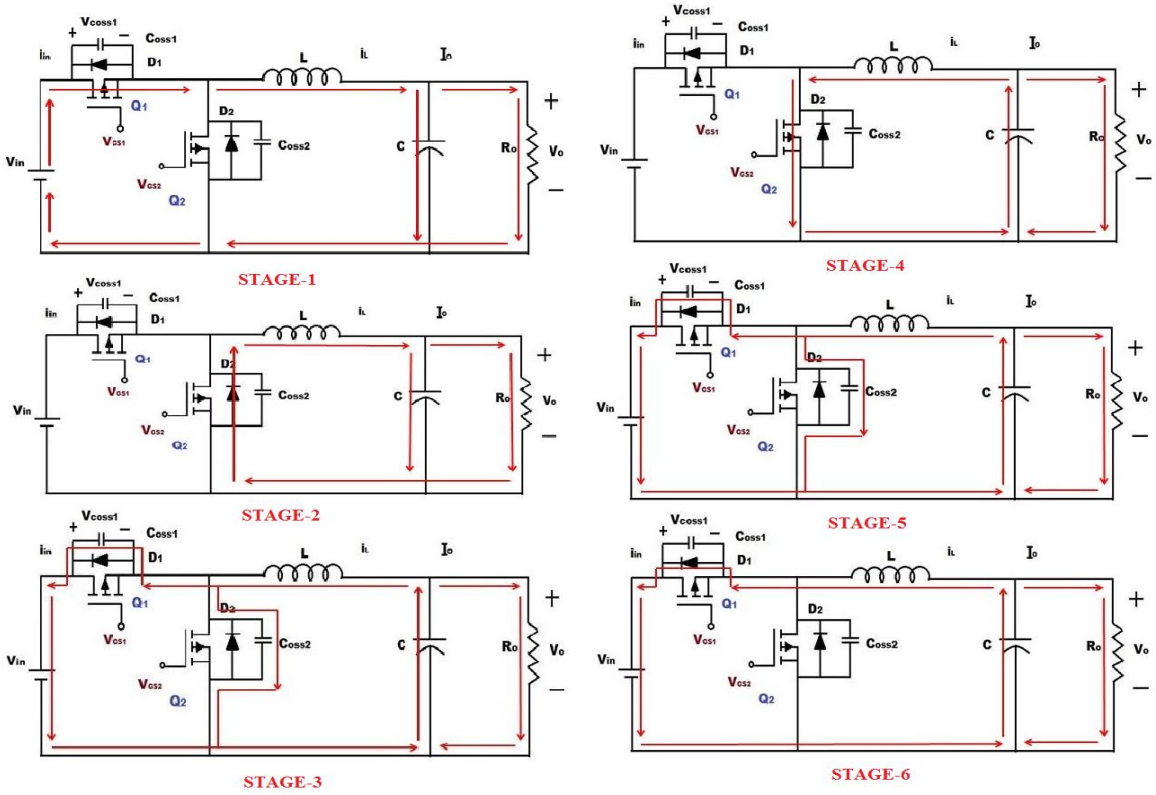

Figure 2. Operating stages of SR Buck Converter (stage1 –stage6)

2.3 Stage 3(t_2- t_3):

The current through the inductor has dropped to zero at the time instant t_2. To avoid energy losses in the SR buck converter, the SR complementary switch Q2 is made to turn OFF. In this stage, the output inductor L begin to resonate with the parasitic capacitors C_{oss} of switches Q1 and Q2 , which makes C_{oss1} to be discharged and other C_{oss2} to be charged. The inductive current $i_L(t)$ and parasitic capacitive voltage v_{Coss1} can be given by:

$$\boldsymbol{i_L(t) = \frac{V_0}{Z} sin\omega(t - t_2)} \quad \textbf{(4)}$$

$$\boldsymbol{v_{Coss1}(t) = (V_{in} - V_0) + V_0 cos\omega(t - t_2)} \quad \textbf{(5)}$$

Where

$$\boldsymbol{Z = \sqrt{\frac{L}{C}} \quad ; \omega = \frac{1}{\sqrt{LC}} \quad ; C = 2C_{OSS} = 2C_{OSS1} = 2C_{OSS2}}$$

2.4 Stage 4(t_3- t_4):

In Stage 4, the main switch Q1 continued to be turned OFF, while the SR switch Q2 is turned ON. As a result, the voltage across the inductor is $v_L = -V_O$, which makes the inductor L to be energized and the inductive current increases linearly in opposite direction.

$$\boldsymbol{i_L(t) = -\frac{V_0}{L}(t - t_3)} \quad \textbf{(6)}$$

$$\boldsymbol{v_{Coss1}(t) = V_{in}} \quad \textbf{(7)}$$

2.5 Stage 5(t_4- t_5):

Stage 5 is the period for resonance. The main switch Q1 and the SR switch Q2, both are made to turn OFF. The SR rectifying switch Q2 is not conducted while the inductor current should be continuous. This current enables C_{oss1} to be discharged and C_{oss2} to be charged, until the voltage across the parasitic capacitor C_{oss1} of switch Q1 is discharged to zero, and the voltage across the parasitic capacitor C_{oss2} of switch Q2 is charged from zero to a voltage V_{in}. The inductive current $i_L(t)$ and parasitic capacitor voltage $v_{Coss1}(t)$ of switch Q1 are calculated as:

$$\boldsymbol{i_L(t) = \frac{V_0}{Z} sin\omega(t - t_4)} \textbf{(8)}$$

$$\boldsymbol{v_{Coss1}(t) = (V_{in} - V_0) + V_0 cos\omega(t - t_4)} \textbf{(9)}$$

Where

$$\boldsymbol{Z = \sqrt{\frac{L}{C}} \quad ; \omega = \frac{1}{\sqrt{LC}} \quad ; C = 2C_{OSS} = 2C_{OSS1} = 2C_{OSS2}}$$

2.6 Stage 6(t_5- t_6):

In Stage 6, the main switch Q1 and the SR rectifying switch Q2 are continued to be turned OFF. Though, the parasitic capacitance C_{oss1} has been already discharged in the previous stage, while C_{oss2} has been discharged by inductive current. The body diode D1 will be conducted. The zero voltage condition of Q1 has been achieved in this stage. $i_L(t)$ and $v_{Coss1}(t)$ of switch Q1 are given as:

$$\boldsymbol{i_L(t) = i_L(t_5) + \frac{(V_{in} - V_O)}{L}(t - t_5)} \textbf{(10)}$$

$$\boldsymbol{v_{Coss1}(t) = 0} \textbf{ (11)}$$

According to the previous explanation, the synchronous buck converter is operated in discontinuous mode (DCM) while operated in light load condition. While the inductive current becomes lesser than zero, the SR rectifying switch Q2 continued to be conducted. This will result in the decrease in conversion efficiency of the synchronous buck converter. The SR rectifying switch Q2 is conducted at the second time in one switching cycle makes the main switch Q1 to be conducted with ZVS and increment the efficiency in light load condition. In conclusion, the control method used here has the following merits. Under heavy loads, SR technique is used to reduce conduction losses whereas under light loads, ZVS technique is achieved to reduce switching losses.

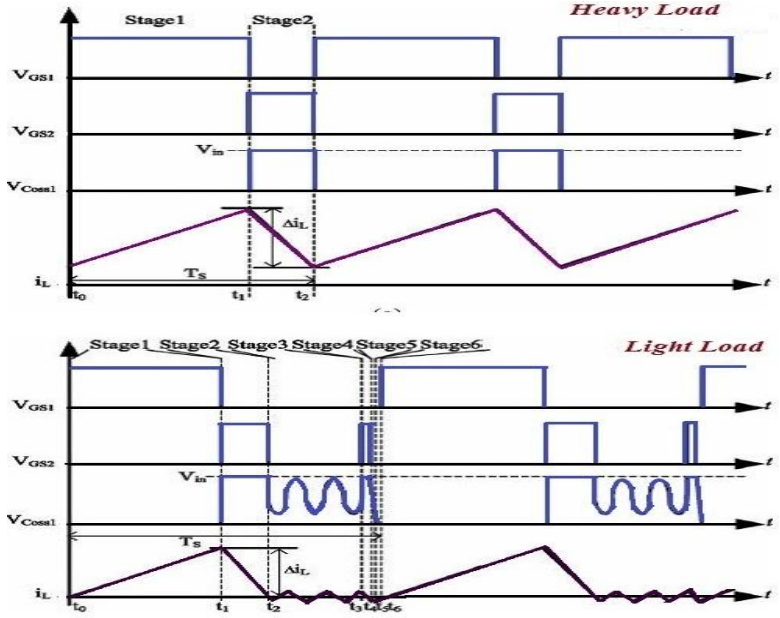

Figure 3.Oscillogram of voltages and inductor current under different load conditions

III. Control Strategy

The control structural circuit diagram of the SR buck converter is shown in Figure 4. It can be also seen that, there is one more zero current detector (ZCD) circuit in the main frame compared with the conventional SR buck converter. The ZCD circuit is mainly used to sense the inductive current and to generate the proper signals for achieving ZVS in light load condition. In the control frame, the PWM controller will be followed by the combination of logic circuit and RC delay circuit. The dead time control between the switches Q1 and Q2 is completed by means of driver circuit. The control structure circuit of SR buck converter comprises of two parts. PWM Controller and ZVS Control logic.

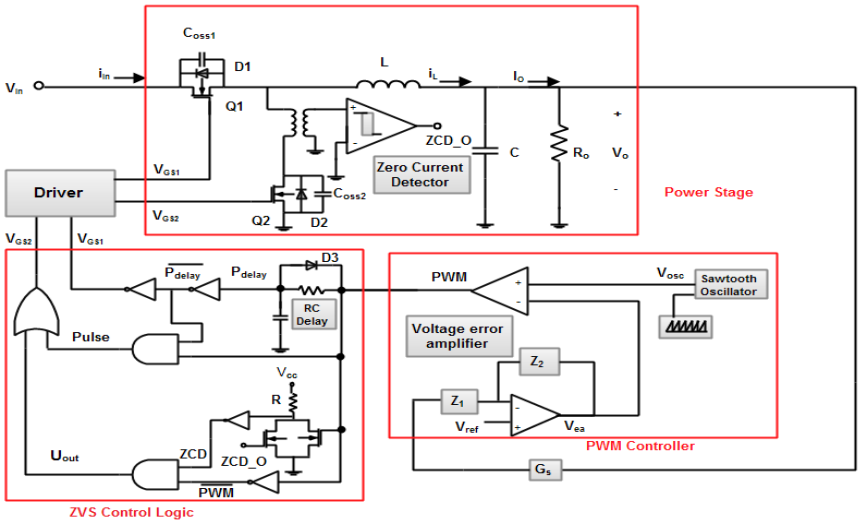

Figure 4. Control circuit structural diagram of an SR buck converter

3.1 PWM Controller

Output voltage is fed back, compared and stabilized with compensated PID error amplifier to get control signal. This control signal is modulated with saw tooth signal to obtain required ***PWM*** signal.

3.2 ZVS control logic

The ***PWM***signal input is first delayed using RC delay (□***t***) after double negation forms $\boldsymbol{V_{GS1}}\cdot\boldsymbol{V_{GS2}}$ is obtained as the OR output of two signals $\boldsymbol{U_{out}}$ and Pulse.Pulse is the AND output of $\overline{\boldsymbol{P_{delay}}}$ and ***PWM*** signal.$\boldsymbol{U_{out}}$is the AND output of **ZCD**and $\overline{\boldsymbol{PWM}}$ signal.. **ZCD** will always be high until inductor current becomes zero. Under heavy load, $\boldsymbol{U_{out}}$is influenced by only ***PWM*** signal.

IV. Simulation Results

Table 1 shows the model parameters of all elements used for simulation.

Table1: Model parameters and their values

No	Parameters	Values
1	Input voltage(V_{in})	12-18V
2	Output voltage(V_O)	5V
3	Switching Frequency(F_s)	10kHZ
4	Output Inductance(L)	0.3mH
5	Output Capacitance(C)	1000μF
6	Electrostatic Resistance(ESR)	100mΩ
7	Maximum Output current	5A

The proposed synchronous buck DC-DC converter with PID compensator control is simulated and the simulation model is presented in the MATLAB Environment.

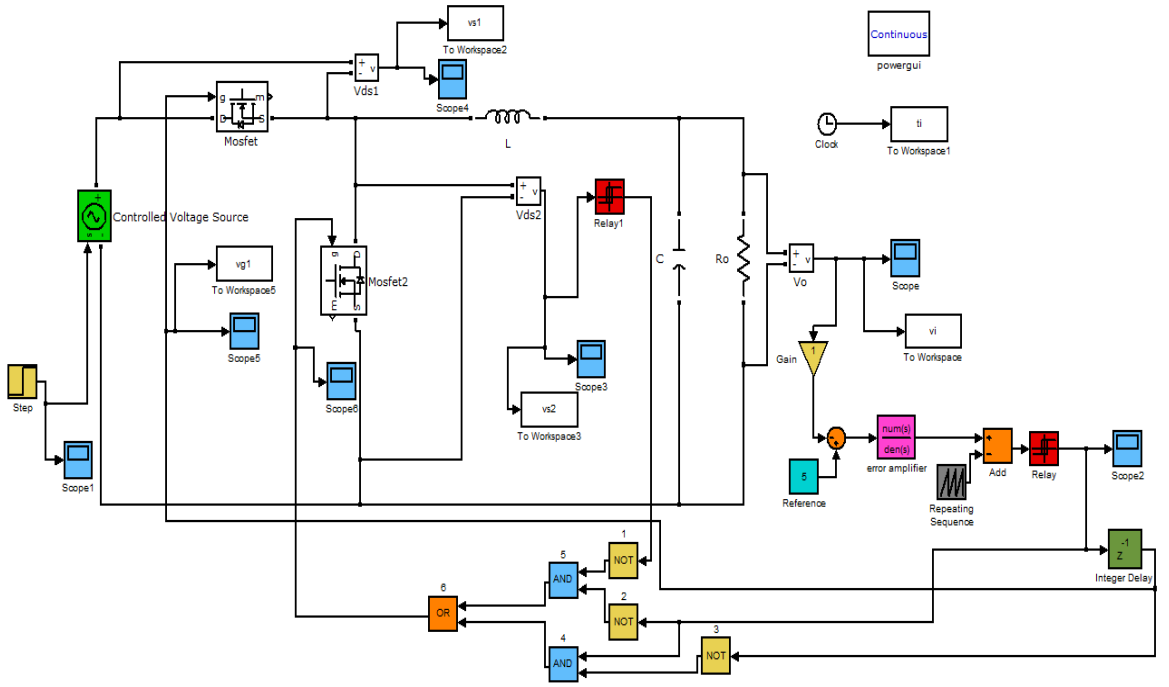

Figure 5. Simulink model for the control of SR buck DC-DC converter with ZVS logic

Figure 5 shows the control strategy for SR buck converter with ZVS logic circuit realized in MATLAB Simulink. The input voltage is varied from 12V to 18V using a controlled voltage source. The input voltage given to the power stage is lowered to 5V at the output. This output voltage is fed back and passed through sensor gain and compared with reference signal in the compensated error amplifier (PID compensator)[24] with a transfer function as given by H(S).

$$\boldsymbol{H(s)} = \frac{(\mathbf{1}+\boldsymbol{sR_{C1}C_{C1}})\left(\mathbf{1}+\boldsymbol{sC_{f3}}\left(\boldsymbol{R_{f1}}+\boldsymbol{R_{f3}}\right)\right)}{\boldsymbol{sR_{f1}C_{C1}}(\mathbf{1}+\boldsymbol{sR_{C1}C_{C2}})(\mathbf{1}+\boldsymbol{sR_{f3}C_{f3}})} = \frac{(\mathbf{1}+\mathbf{0.00145806}\boldsymbol{s}+\mathbf{5.3148368}\boldsymbol{e^{-7}s^2})}{(\mathbf{0.0003329}\boldsymbol{s}+\mathbf{0.00145806}\boldsymbol{e^{-7}s^2}+\mathbf{5.3148368}\boldsymbol{e^{-12}s^3})}$$

The control signal obtained from the compensated error amplifier is then modulated with saw tooth signal to generate PWM. This generated PWM is applied as the input to the ZVS control logic circuit. The gating control signals for both switches are the outputs of ZVS control logic.

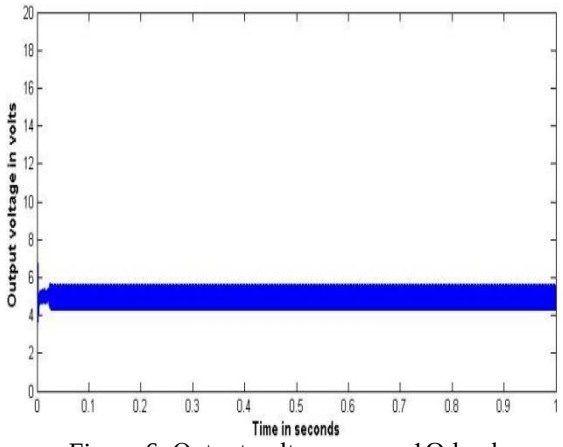

Figure 6: Output voltage across 1Ω load

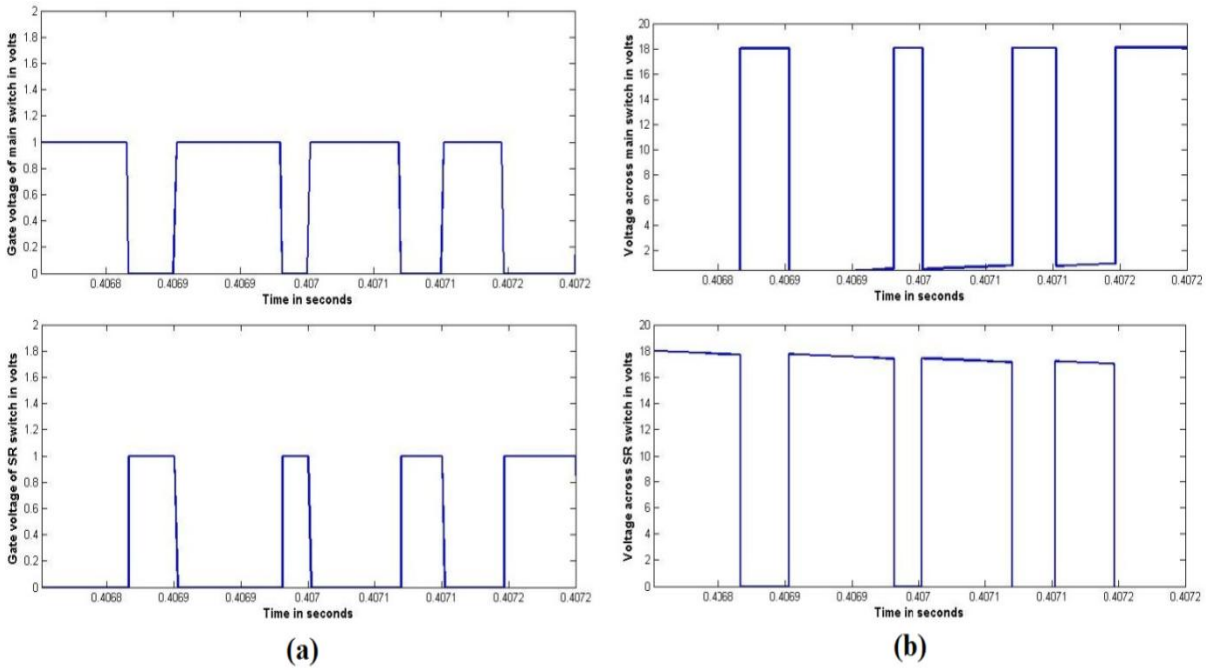

Figure 7: Gate voltages (a) and Drain-sourcevoltages (b) for main switch Q1 and SR witch Q2 for 1Ω load resistor

The figure 6 and figure 7 shows the variations of output voltages,switch voltages and gate voltages with respect to time in case of SR buck converter with voltage mode control and voltage error amplifier using ZVS control logic for load resistance of 1Ω respectively. Since the load resistance is low and this operating condition is also termed as heavy load condition.In figure 6, it can be seen that gate voltageof main switch and drain-source voltage of main switch is complementary.That means, the ZVS condition of the main switch is achieved.

The load resistance is increased by 100 times to obtain the simulation results at light load conditions.The figure 8 and figure 9shows the variations of output voltages, switch voltages and gate voltages with respect to time in case of SR buck converter with voltage mode control and voltage error amplifier using ZVS control logic for load resistance of 100Ω. Since the load resistance is high and this operating condition is also termed as light load condition. In figure 9, it can be also seen that gate voltage of main switch and drain-source voltage of main switch is complementary. That means, the ZVS condition of the main switch is also achieved in light load condition.

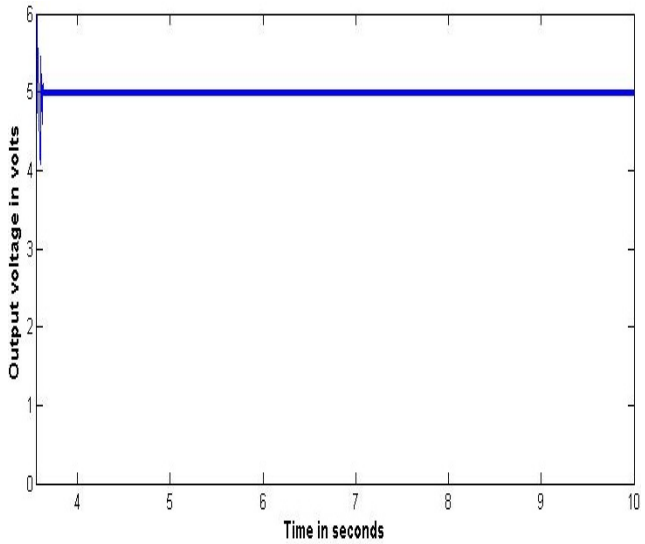

Figure 8. Output voltage across 100Ω load

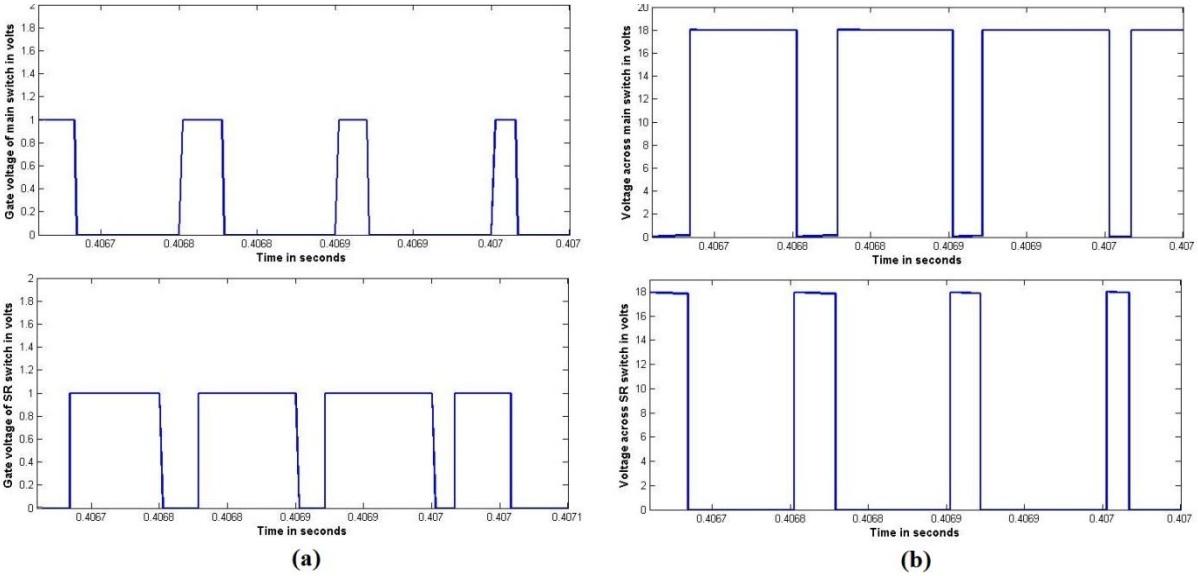

Figure 9.Gate voltages (a) and Drain- source voltages (b) for main switch Q1 and SR witch Q2 for 100Ω load resistor

Thus, under light and heavy load conditions, the output voltage is maintained regulated at 5V for even input voltage variation from 12 to 18V. The ZVS condition of the main switch helps in reducing switching losses with improved light load efficiency.

V. Conclusions

The control technique with PID compensator network and ZVS control logicapplicable to an SR buck converter under any operating load condition is designed and simulated by analyzing the converter operating modes. Under heavy load condition, SR technique (SR configuration itself) is used to reduce conduction losses achieving better normal mode performance while under light load conditions; ZVS technique is achieved to reduce the switching losses. This is the control strategy adopted for SR buck converter to operate under any load conditions. This control method has two advantages. First, due to the SR technique, the diode of output rectifier can be replaced by a MOSFET. This will help to reduce conduction losses and increase the conversion efficiency of the converter. Second, when the converter is operated in light load condition, ZVS will be achieved successfully without any auxiliary switch or passive components(R, L, and C). In other words, there is no need to add extra cost in the converter, and thus the conversion efficiency of the converter can also be increased in light load condition. This new control strategy with Type III-A PID compensator and ZVS logic has better conversion efficiency than the conventional control technique in light load condition. Simulation is done showing the voltage control of SR buck converter stabilized with Type III-A proportional-integral-derivative (PID) compensator and ZVS control logic circuit using MATLAB/SIMULINK.

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