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Analysis Of 3C-Sic Double Implanted MOSFET With Gaussian Profile Doping In The Drift Region For High Breakdown Voltage

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ABSTRACT*: The present work aims at the design of 3C-SiC Double Implanted Metal Oxide Semiconductor Field Effect Transistor (DIMOSFET) with Gaussian doping profile in drift region for high breakdown voltages. By varying the device height 'h', function constant m and peak concentration N_0, analysis has been done for an optimum profile for high breakdown voltage. With Gaussian profile peak concentration $N_0 = 10^{16}\ cm^{-3}$ at drain end and m as $1.496 \times 10^{-2} cm$, highest breakdown voltage of 6.84kV has been estimated with device height of 200µm.*

Keywords - *Avalanche breakdown voltage, DIMOSFET, Punch through breakdown voltage, Silicon carbide (SiC).*

I. Introduction

Silicon carbide (SiC) is a potential compound semiconductor for high temperature, high frequency and high power electronic applications due of its wide band gap, high value of saturated drift velocity, high breakdown electric field and high thermal conductivity. SiC exists in different polytypes where difference between these lies in the stacking order between the double layers of carbon and silicon atoms. Among other polytypes, the most important are cubic (3C) and hexagonal (4H and 6H) forms. The distinct polytypes differ in both band gap energies and electronic properties. Thus band gap varies with the polytype from 2.2eV for 3C-SiC over 3.0eV for 6H-SiC to 3.2eV for 4H-SiC. 3C- SiC polytype has many advantages compared to other polytypes such as isotropic electron Hall mobility [1] (due to low density of interface states), smaller band gap that permits "inversion" at lower electric field strengths. Also the interface states observed in 6H-SiC and 4H-SiC are located in the band gap close to conduction band edge, limiting the transport of electrons in the channel [2]. Due to the smaller band gap of 3C-SiC, observed interface states are located in conduction band and thus have no effect on the transport properties of the channel .The 3C-SiC polytype has lower critical electric field value due to smaller band gap. Thus for a given blocking voltage, specific junction capacitance will be lower in the 3C-SiC devices as compared to the 4H-SiC and 6H-SiC due of lower drift region doping[2]. This is an advantage for the high speed MOSFETs.

However research pertaining to SiC power devices and their practical application has been held back by lack of reproducible techniques to grow semiconductor quality single crystals and epilayers. Over the last few years considerable progress has been made mainly in the development of 4H and 6H - SiC wafers and the related devices. However, there is a deviation of the SiC device parameters from theoretical expectations and cost of these wafers also remains high. So there is a significant interest in low cost, large size 3C-SiC wafers for various microelectronic applications. A lot of work is being done in the area of structural characterization and crystal growth in order to get defect free 3C-SiC wafers [3-8]. Till now, large mono-crystal 3C-SiC substrates (at least 200 µm thick, six inch in diameter, after removing the Si base layer), can be manufactured with the help of a new process originated by HOYA Corporation, Japan [9]. Thus, in this paper height of device does not exceed beyond 200 µm. HOYA's 3C-SiC substrate has the same geometry as typical Silicon wafers and can be used in conventional Silicon semiconductor device production lines without hardware modifications.

II. Analysis of DIMOSFET for high breakdown voltage

The fabrication of DIMOSFET structure is normally done by using planar diffusion technology with a gate such as poly silicon. In these devices, the edge of the poly silicon gate serves as a common window for the diffusion of p-base and n+ - source regions. Fig.1 shows a cross section of a power DIMOSFET structure. Difference in the lateral diffusion between the p-base and n+ source region defines the surface channel region [10]. The forward blocking capability is achieved by the p-n junction between the p-base region and the n-drift region. During the device operation, a fixed potential to the p-base region is provided by the connection of base to the source metal through a break in the n+ source region. By applying a positive bias to the drain and short-circuiting the gate to the source, the p-base and n-drift region junction becomes reverse-biased thus supporting the drain voltage by the extension of a depletion layer on both sides of the junction [10]. However, the depletion layer extends primarily into the n-drift region due to its lower doping level as compared to p-base region. A

conductive path extending between the n+ - source region and the n-drift region is formed by applying positive bias to the gate electrode. The application of a positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel.

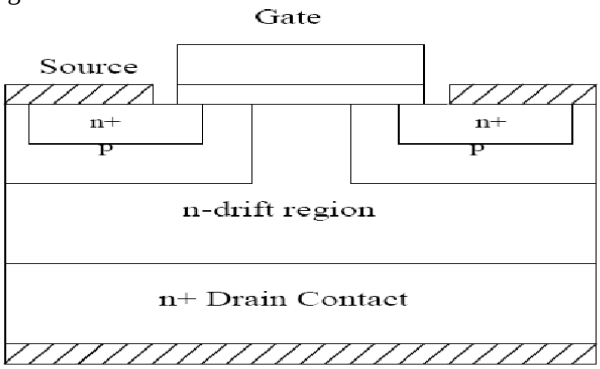

Fig.1. Structure of basic DIMOSFET [10]

Doping profiles used in semiconductor industry commercially normally employ non-linearly graded profiles inside semiconductor layers. Gaussian or Complementary Error Function distribution is the most preferred profiles for improved results [11]. This work analyses the device structure of vertical DIMOSFET with Gaussian Profile doping in the drift region as shown in Fig.2. The Gaussian profile has been adopted with the peak lying at the drain end of the device and the doping concentration falls to small values near the n-drift region and p-base junction. This procedure provides a low parasitic series resistance near the drain and a large depletion region in the drift region near the junction.

The equation for Gaussian profile is written as [11]:

$$G(x) = N_0 \, exp^{-\left(\frac{h-x}{m}\right)^2} \quad (1)$$

N_0 is the maximum concentration at the drain end, 'h' is device height, m is a function constant. The depletion region width at any given reverse voltage V_R can be obtained by solving the Poisson's equation for the system For the Gaussian function G(x), the Poisson's equation becomes [11]:

$$-\partial^2 V/\partial^2 x = (e/\varepsilon_s)\, G(x) = (eN_0/\varepsilon_s)\, exp^{-\left(\frac{h-x}{m}\right)^2} \quad (2)$$

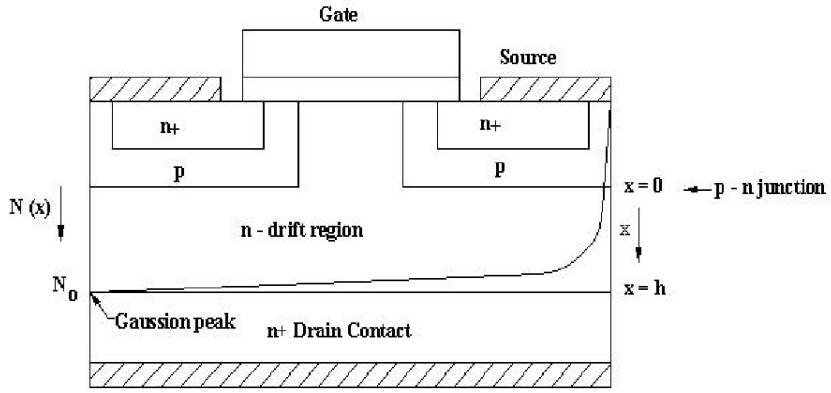

Fig. 2. Cross-sectional structure of DIMOSFET showing Gaussian profile in the drift region [11]

ε_s is relative permittivity of medium and e is the charge of an electron.

Solving the above equation for voltage V with proper initial conditions and first order error function approximation [11] :

$$-V(x) = (eN_0/\varepsilon_s)\ [(x^4/12m^2) - (h\,x^3/3\,m^2) - (x^2/2)\,(1 - h^2/m^2)] \quad (3)$$

At x=W, the depletion region width under a reverse bias V_R is given as:

$$V(W) = V_{bi} + V_R$$

where V_{bi} is the built-in potential.

Substituting x=W and V (W) = $-V_R$ (as $V_R >> V_{bi}$) in eq. (3), gives [11]:

$$[(W^4/12m^2) - (h\,W^3/3\,m^2) - (W^2/2)(1 - h^2/m^2)] - (\varepsilon_s\, V_R/eN_0) = 0 \quad (4)$$

Above equation has been used to calculate the depletion region width W at a given reverse bias voltage V_R between the p-body and n-drift region of DIMOSFET.

III. Punch through breakdown voltage V_{BPT} and Avalanche breakdown voltage V_{BAV}

The device height has been set at 200µm and 150µm for various values of m and doping level in the drift region. Analysis of equation (4) has been done in order to increase the reverse voltage V_R to a value for which maximum depletion width does not go beyond the device height. That maximum value of reverse voltage is taken as Punch through breakdown voltageV_{BPT} .

Avalanche breakdown voltage V_{BAV} has been calculated by approximating Gaussian profile as linearly graded profile in the drift region. This approximation is valid for large device heights as considered here. For linearly graded profile avalanche breakdown voltage is given by [12]:

$$V_{BAV} = (2/3)\, E_c\, W' \quad (5)$$

where E_c is the critical field which is given by [12]:

$$E_c = (e\, \alpha\, W'^2/8\square_s) \quad (6)$$

where α is concentration gradient, W' is depletion region width at breakdown.

Concentration gradient α was obtained by taking the difference of carrier concentrations at the source and drain end and dividing it by the device height 'h'. Calculations of two breakdown voltages (punch through and avalanche) are done by using same depletion region width.

IV. Results and Calculations

Calculations of punch through breakdown voltages (V_{BPT}) and avalanche breakdown voltages (V_{BAV}) were made for three Gaussian profiles. Table1 shows three results with critical field E_c and concentration gradient α.

Table 1. Results of breakdown voltages (V_{BPT} and V_{BAV}) for various profiles

Profiles	Device Height (µm)	m (µm)	N_0 (cm^{-3})	α (cm^{-4})	E_C (V/cm)	V_{BPT} (kV)	V_{BAV} (kV)
1.	200	100	0.67×10^{15}	3.29×10^{16}	3.08×10^{5}	25	4.106
2.	150	78	1.1×10^{15}	7.16×10^{16}	3.767×10^{5}	19.6	3.767
3.	200	149.6	10^{16}	4.17×10^{17}	10.09×10^{5}	25	6.84

The Gaussian profiles that are given above are shown in Fig. 3 with peak concentration of N_0 . Doping level is minimum near the source end and maximum at the drain end.

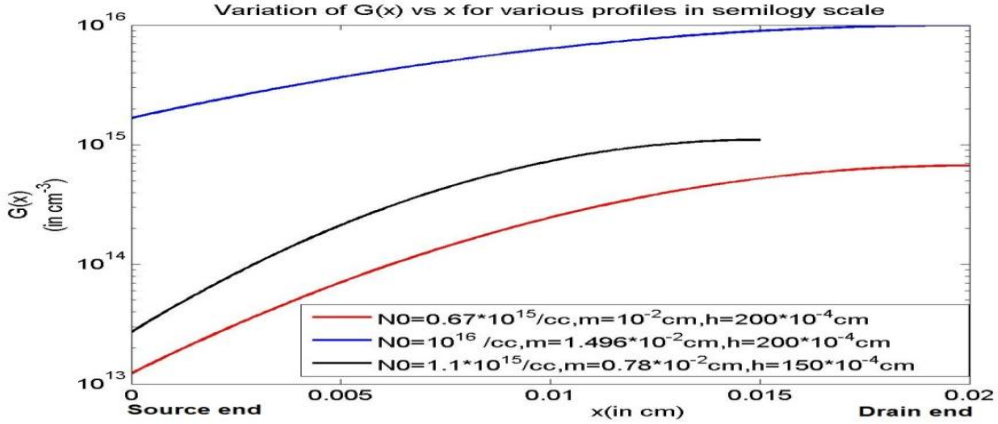

Fig.3. Variation of G(x) vs. x for various profiles in semi-log scale

For the first and third profile, the drain to source distance or device height 'h' has been set as 200µm. The second profile utilizes a device height of 150µm, as increasing the device height beyond this thickness leads to a decline in the avalanche breakdown voltage. The analysis of depletion region width and reverse voltage for all three profiles is shown in Fig. 4. To a first approximation the relationship between the two can be considered as almost linear over the range of 0 to 25 kV for a device height of 150 to 200µm. A slight amount of non linearity seems to exist in three profiles for reverse voltages lying between 0 to 5 kV and 20 to 25 kV.

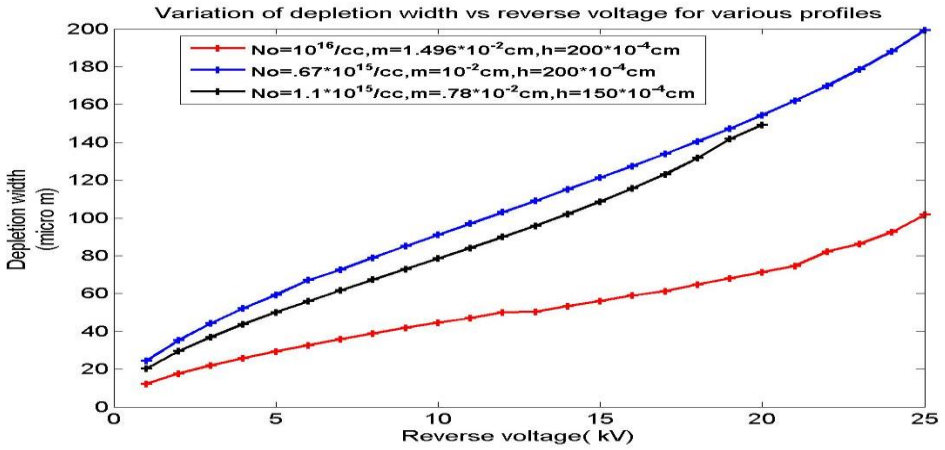

Fig.4. Variation of Depletion region width vs. Reverse voltage for the three profiles

Hence it is clear that profile 3 with a device height of 200 µm, m = 1.496× 10^{-2}cm, N_0 = 10^{16}/cc, α = 4.17× 10^{17} cm^{-4} is expected to provide the highest avalanche breakdown voltage of 6.84 kV corresponding to a punch through voltage of 25 kV. Analysis quoted above gives the breakdown voltage of 6.84 kV for Gaussian profile in profile 3 but the design procedure does point to one disadvantage that there is significant difference in the values of punch through breakdown voltage V_{BPT} and avalanche breakdown voltage V_{BAV} in all the profiles that have been studied.

V. Conclusion

Analysis of different profiles have been done to calculate maximum breakdown voltage for the device as shown in Table 1.For the drift region height h=200µm, N_0 = 10^{16}/cm^3 and m = 1.496× 10^{-2} cm, the punch through breakdown voltage was found to be 25kV and corresponding avalanche breakdown voltage was calculated as 6.84kV when Gaussian profile was approximated as linearly graded profile in drift region. So, under the constraints of device height, peak concentration and function constant, the maximum breakdown voltage for the device is estimated as 6.84 kV. It could be seen that avalanche breakdown will occur much before than punch through breakdown. More detailed analysis is required in the use of Gaussian profile in drift region that can yield almost equal values for punch through and avalanche breakdown voltages for 3C-SiC DIMOSFET. Having attained this, it would be advisable to analyze the theory for attaining breakdown voltages far in excess of the avalanche breakdown voltage of 6.84 kV obtained here.

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